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## Yx70 GN20E M/B Schematics Document

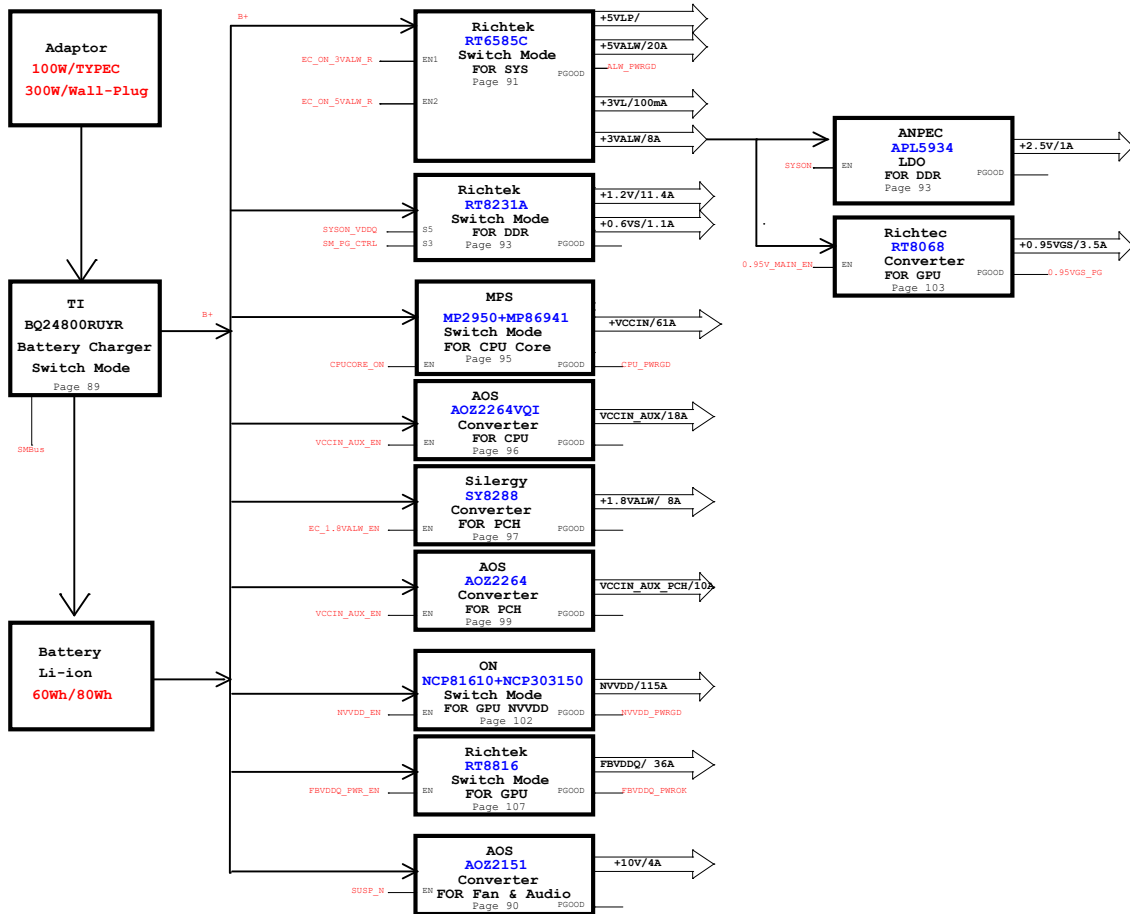
### Alder Lake P-Processor with DDR5 + NV GN20-E GPU

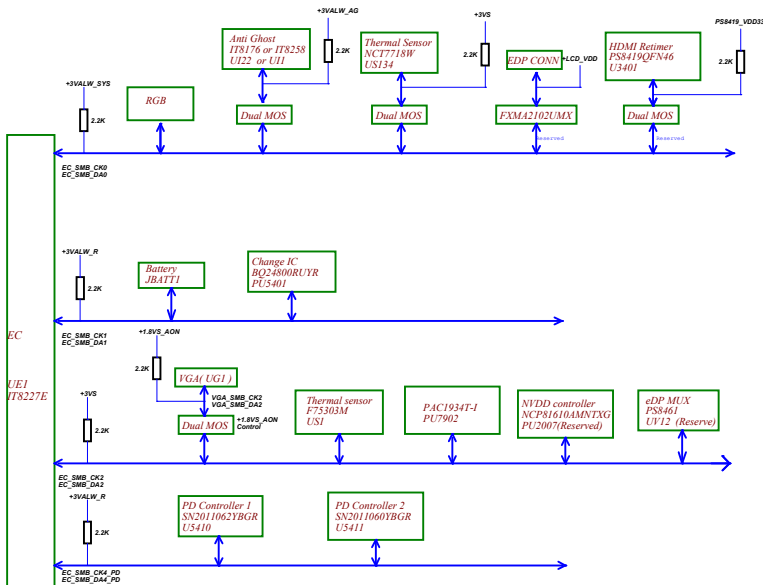
2021-11-29

REV : A0

Security Classification	LC Future Center Secret Data		Title		
Issued Date	2018/08/02	Deciphered Date	2018/08/02		Cover Page
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			Custom	y550	A0
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SMBUS Control Table

	ADDRESS	W0	W1	W2	W3	W4	W5	W6	W7	W8	W9	W10	W11	W12	W13	W14	W15	W16	W17	W18	W19	W20	W21	W22	W23	W24	W25	W26	W27	W28	W29	W30	W31	W32	W33	W34	W35	W36	W37	W38	W39	W40	W41	W42	W43	W44	W45	W46	W47	W48	W49	W50	W51	W52	W53	W54	W55	W56	W57	W58	W59	W60	W61	W62	W63	W64	W65	W66	W67	W68	W69	W70	W71	W72	W73	W74	W75	W76	W77	W78	W79	W80	W81	W82	W83	W84	W85	W86	W87	W88	W89	W90	W91	W92	W93	W94	W95	W96	W97	W98	W99	W100	W101	W102	W103	W104	W105	W106	W107	W108	W109	W110	W111	W112	W113	W114	W115	W116	W117	W118	W119	W120	W121	W122	W123	W124	W125	W126	W127	W128	W129	W130	W131	W132	W133	W134	W135	W136	W137	W138	W139	W140	W141	W142	W143	W144	W145	W146	W147	W148	W149	W150	W151	W152	W153	W154	W155	W156	W157	W158	W159	W160	W161	W162	W163	W164	W165	W166	W167	W168	W169	W170	W171	W172	W173	W174	W175	W176	W177	W178	W179	W180	W181	W182	W183	W184	W185	W186	W187	W188	W189	W190	W191	W192	W193	W194	W195	W196	W197	W198	W199	W200	W201	W202	W203	W204	W205	W206	W207	W208	W209	W210	W211	W212	W213	W214	W215	W216	W217	W218	W219	W220	W221	W222	W223	W224	W225	W226	W227	W228	W229	W230	W231	W232	W233	W234	W235	W236	W237	W238	W239	W240	W241	W242	W243	W244	W245	W246	W247	W248	W249	W250	W251	W252	W253	W254	W255	W256	W257	W258	W259	W260	W261	W262	W263	W264	W265	W266	W267	W268	W269	W270	W271	W272	W273	W274	W275	W276	W277	W278	W279	W280	W281	W282	W283	W284	W285	W286	W287	W288	W289	W290	W291	W292	W293	W294	W295	W296	W297	W298	W299	W300	W301	W302	W303	W304	W305	W306	W307	W308	W309	W310	W311	W312	W313	W314	W315	W316	W317	W318	W319	W320	W321	W322	W323	W324	W325	W326	W327	W328	W329	W330	W331	W332	W333	W334	W335	W336	W337	W338	W339	W340	W341	W342	W343	W344	W345	W346	W347	W348	W349	W350	W351	W352	W353	W354	W355	W356	W357	W358	W359	W360	W361	W362	W363	W364	W365	W366	W367	W368	W369	W370	W371	W372	W373	W374	W375	W376	W377	W378	W379	W380	W381	W382	W383	W384	W385	W386	W387	W388	W389	W390	W391	W392	W393	W394	W395	W396	W397	W398	W399	W400	W401	W402	W403	W404	W405	W406	W407	W408	W409	W410	W411	W412	W413	W414	W415	W416	W417	W418	W419	W420	W421	W422	W423	W424	W425	W426	W427	W428	W429	W430	W431	W432	W433	W434	W435	W436	W437	W438	W439	W440	W441	W442	W443	W444	W445	W446	W447	W448	W449	W450	W451	W452	W453	W454	W455	W456	W457	W458	W459	W460	W461	W462	W463	W464	W465	W466	W467	W468	W469	W470	W471	W472	W473	W474	W475	W476	W477	W478	W479	W480	W481	W482	W483	W484	W485	W486	W487	W488	W489	W490	W491	W492	W493	W494	W495	W496	W497	W498	W499	W500	W501	W502	W503	W504	W505	W506	W507	W508	W509	W510	W511	W512	W513	W514	W515	W516	W517	W518	W519	W520	W521	W522	W523	W524	W525	W526	W527	W528	W529	W530	W531	W532	W533	W534	W535	W536	W537	W538	W539	W540	W541	W542	W543	W544	W545	W546	W547	W548	W549	W550	W551	W552	W553	W554	W555	W556	W557	W558	W559	W560	W561	W562	W563	W564	W565	W566	W567	W568	W569	W570	W571	W572	W573	W574	W575	W576	W577	W578	W579	W580	W581	W582	W583	W584	W585	W586	W587	W588	W589	W590	W591	W592	W593	W594	W595	W596	W597	W598	W599	W600	W601	W602	W603	W604	W605	W606	W607	W608	W609	W610	W611	W612	W613	W614	W615	W616	W617	W618	W619	W620	W621	W622	W623	W624	W625	W626	W627	W628	W629	W630	W631	W632	W633	W634	W635	W636	W637	W638	W639	W640	W641	W642	W643	W644	W645	W646	W647	W648	W649	W650	W651	W652	W653	W654	W655	W656	W657	W658	W659	W660	W661	W662	W663	W664	W665	W666	W667	W668	W669	W670	W671	W672	W673	W674	W675	W676	W677	W678	W679	W680	W681	W682	W683	W684	W685	W686	W687	W688	W689	W690	W691	W692	W693	W694	W695	W696	W697	W698	W699	W700	W701	W702	W703	W704	W705	W706	W707	W708	W709	W710	W711	W712	W713	W714	W715	W716	W717	W718	W719	W720	W721	W722	W723	W724	W725	W726	W727	W728	W729	W730	W731	W732	W733	W734	W735	W736	W737	W738	W739	W740	W741	W742	W743	W744	W745	W746	W747	W748	W749	W750	W751	W752	W753	W754	W755	W756	W757	W758	W759	W760	W761	W762	W763	W764	W765	W766	W767	W768	W769	W770	W771	W772	W773	W774	W775	W776	W777	W778	W779	W780	W781	W782	W783	W784	W785	W786	W787	W788	W789	W790	W791	W792	W793	W794	W795	W796	W797	W798	W799	W800	W801	W802	W803	W804	W805	W806	W807	W808	W809	W810	W811	W812	W813	W814	W815	W816	W817	W818	W819	W820	W821	W822	W823	W824	W825	W826	W827	W828	W829	W830	W831	W832	W833	W834	W835	W836	W837	W838	W839	W840	W841	W842	W843	W844	W845	W846	W847	W848	W849	W850	W851	W852	W853	W854	W855	W856	W857	W858	W859	W860	W861	W862	W863	W864	W865	W866	W867	W868	W869	W870	W871	W872	W873	W874	W875	W876	W877	W878	W879	W880	W881	W882	W883	W884	W885	W886	W887	W888	W889	W890	W891	W892	W893	W894	W895	W896	W897	W898	W899	W900	W901	W902	W903	W904	W905	W906	W907	W908	W909	W910	W911	W912	W913	W914	W915	W916	W917	W918	W919	W920	W921	W922	W923	W924	W925	W926	W927	W928	W929	W930	W931	W932	W933	W934	W935	W936	W937	W938	W939	W940	W941	W942	W943	W944	W945	W946	W947	W948	W949	W950	W951	W952	W953	W954	W955	W956	W957	W958	W959	W960	W961	W962	W963	W964	W965	W966	W967	W968	W969	W970	W971	W972	W973	W974	W975	W976	W977	W978	W979	W980	W981	W982	W983	W984	W985	W986	W987	W988	W989	W990	W991	W992	W993	W994	W995	W996	W997	W998	W999	W1000	W1001	W1002	W1003	W1004	W1005	W1006	W1007	W1008	W1009	W1010	W1011	W1012	W1013	W1014	W1015	W1016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GN20x-E GPIO

GPIO	I/O	GPIO Name	Function Description	Net name	I/O Termination
GPIO0	OUT	NVDD_PWM_VID	PWM Output to control NVDD	NVDD_PWM_VID	
GPIO1	OUT	GC6:GC6_FB_EN	FB Enable for GC6	FB_GC6_EN	(10K PD)
GPIO2	IN	GC6:GPU_EVENT*	Wake the GPU from GC6 state	GPU_EVENT#_R	(10K PU)
GPIO3	OUT	DISP_MUX_CNTL	Display MUX control signal	GPU_MUX_CNTL	(10K PD)
GPIO4	OUT	MSVDD_EN	GPU power sequencing for GC6 --MSVDD_EN	GPIO4_GC6_MSVDD_EN	(10K PU)
GPIO5	OUT	FRAME_LOCK*	Active low Frame Lock for NVSR panel	UNUSED	
GPIO6	OUT	NVDD_PSI*	Phase Shedding, NVDD_PSI	NVDD_PSI	(10K PU) <b>RSVD</b>
GPIO7	OUT	LCD_BL_PWM	LCD Panel Backlight PWM	GPU_EDP_PWM	(100K PD)
GPIO8	OUT	MEM_VDD_CTL	Memory voltage Control	FBVDDQ_SEL	(10K PD)
GPIO9	I/O	THERM_ALERT*	Active Low Thermal Alert	VGA_ALERT#	(10K PU)
GPIO10	OUT	MEM_VREF_CTL	Memory VREF Control	MEM_VREF_CTL	(100K PD)
GPIO11	OUT	LCD_VDD	LED Panel power enable	GPU_EDP_ENVDD	(10K PD)
GPIO12	IN	PWR_LEVEL	AC power detect or power supply overdraw input	VGA_AC_DET_R	(10K PU)
GPIO13	IN	IGPU_BL_EN	Signal indicating when the IGPU has EN the BL	IGPU_EDP_ENBK_L	(100K PU)
GPIO14	IN	HPD_IFPA*	Hot Plug Detect for IFPA	IFPA_HPD	(10K PU)
GPIO15	IN	HPD_IFPB*	Hot Plug Detect for IFPB	IFPB_HPD	(10K PU)
GPIO16	OUT	DISP_MUX_PWM_CNTL	Allows switching the PWM between IGPU & DGPU	PWM_SW_SELECT	(10K PD)
GPIO17	IN	HPD_IFPD*	Hot Plug Detect for IFPD	GPU_EDP_HPD	(10K PU)
GPIO18	IN	HPD_IFPE*	Hot Plug Detect for IFPE	UNUSED	
GPIO19	OUT	UNUSED			
GPIO20	OUT	UNUSED			
GPIO21	OUT	LCD_BLEN	LCD Panel Backlight Enable	GPU_EDP_ENBK_L	(100K PD)
GPIO22	OUT	ADC_MUX_SEL	OVRM MUX Input SEL	ADC_MUX_SEL	(2.2K PU)
GPIO23	OUT	UNUSED			
GPIO24	IN	HPD_IFPF*/USBC_HPD* or DONGLE_DET*	Hot Plug Detect for IFPF or USBC	UNUSED	
GPIO25	OUT	FBVDD_PSI	Turns off phases of the Frame buffer power supply	FBVDDQ_PSI	(5.1K PU)
GPIO26	OUT	ROM_WP* FP_FUSE N18P-G61-A Control FP_FUSE	Connect to WP pin of the GPU EEPROM	GPIO26_ROM_WP GPIO26_FP_FUSE	(10K PD) (10K PD) <b>RSVD</b>
GPIO27	IN	HPD_IFPC*	Hot Plug Detect for IFPC	IFPC_HPD	(10K PU)
GPIO28	OUT	MSVDD_PWM_VID	PWM Ooutput to CNTL MSVDD	UNUSED	
GPIO29	OUT	NVDD_EN	NVDD Enable <b>RSVD</b>	GPIO29_NVDD_EN	(100K PU) <b>RSVD</b>
GPIO30	OUT	MSVDD_PSI*	Phase Shedding	UNUSED	

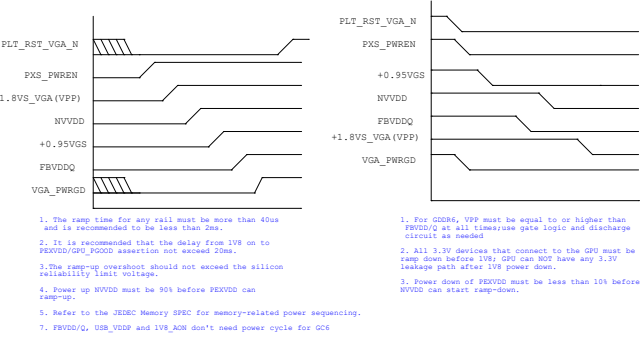
H=High: Tied to 1.8V  
M=Middle: Tied to 0.9V  
L=Low: Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	GN20x-E VRAM
L	L	L	0 (0x0000)	Samsung K4Z803258C-HC14
L	L	H	1 (0x0001)	Micron MT61H256M32JE-14-A
L	H	L	2 (0x0002)	Hynix H56C8H24AIR-S2C
L	H	H	3 (0x0003)	
H	L	L	4 (0x0004)	
H	L	H	5 (0x0005)	
H	H	L	6 (0x0006)	
H	H	H	7 (0x0007)	
L	L	M	8 (0x0008)	
L	M	L	9 (0x0009)	Samsung (or E7) K4ZAF3258M-HC 14
L	M	H	10 (0x000A)	
L	H	M	11 (0x000B)	
M	L	L	12 (0x000C)	
M	L	H	13 (0x000D)	

FS\_OVERT# FUNCTION

ROM_SO	ROM_SI	ROM_SCLK	FS_OVERT# FUNCTION
L	L	H	FS_OVERT# function ENABLE
L	L	L	FS_OVERT# function DISABLE Reserved, do not configure

GN20x-E Power Sequence



STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

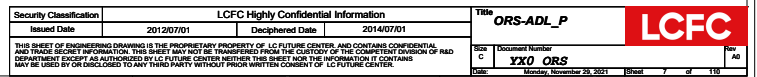
- 1:SMB\_ALT\_ADDR ENABLE
- 0:SMB\_ALT\_ADDR DISABLE
- 1:DEVID\_SEL REBRAND
- 0:DEVID\_SEL ORIGINAL
- 1:PCIE\_CFG LOW POWER
- 0:PCIE\_CFG HIGH POWER
- 1:VGA\_DEVICE ENABLE
- 0:VGA\_DEVICE DISABLE

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Size	C	Document Number	Y550	
Ver	4.0	Rev	4.0	
File	Memory	Version	25	2021
Printed	5	of	116	

[illegible]

ROM Structure Control Table	
ROM	ROM structure
0	ROM 0
1	ROM 1
2	ROM 2
3	ROM 3
4	ROM 4
5	ROM 5
6	ROM 6
7	ROM 7
8	ROM 8
9	ROM 9
10	ROM 10
11	ROM 11
12	ROM 12
13	ROM 13
14	ROM 14
15	ROM 15
16	ROM 16
17	ROM 17
18	ROM 18
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148	ROM 148
149	ROM 149
150	ROM 150
151	ROM 151
152	ROM 152
153	ROM 153
154	ROM 154
155	ROM 155
156	ROM 156
157	ROM 157

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Document Number		YX0 ORS		LCFC	
Date		Monday, November 25, 2021		Page 2 of 16	



26 DDRB\_DQ[0..63]  DDRB\_DQ[0..63]

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UC10

BMAP REV = ?

EMAP\_REV = ?

[illegible]

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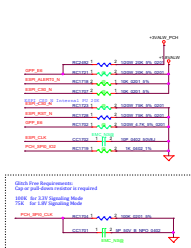
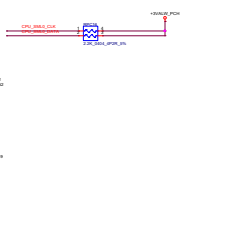
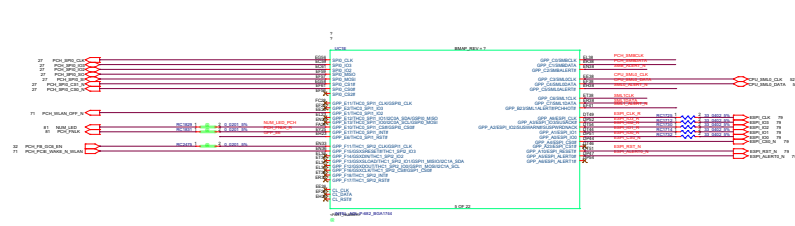
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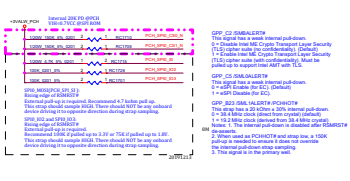
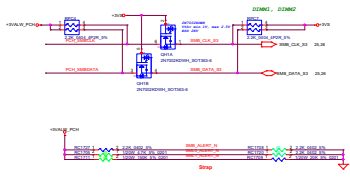
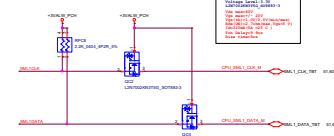
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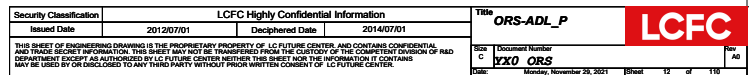
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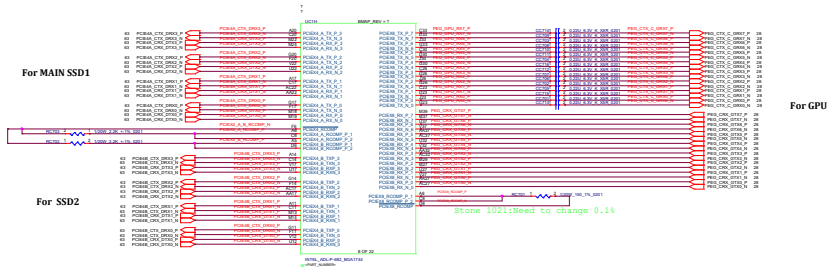
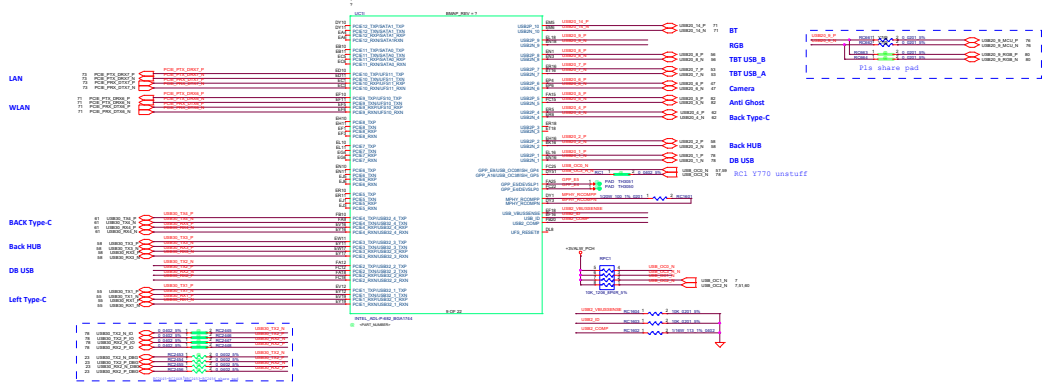


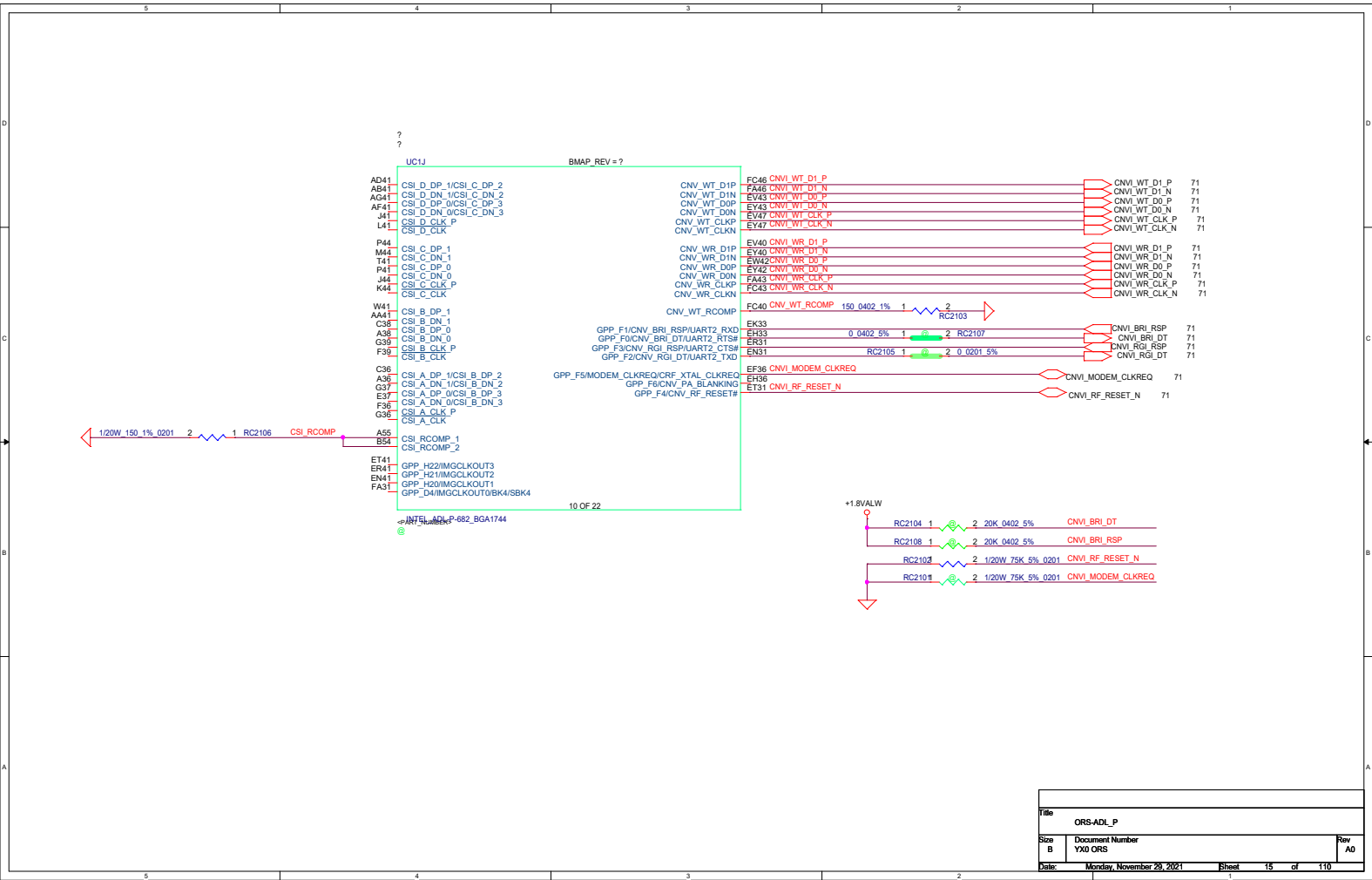
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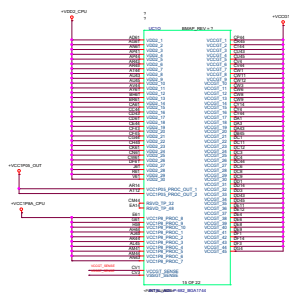
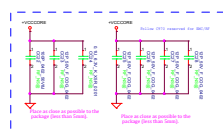
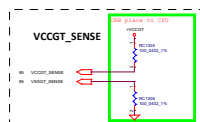
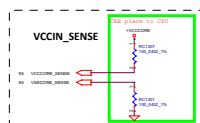
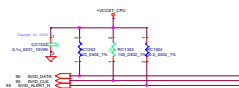
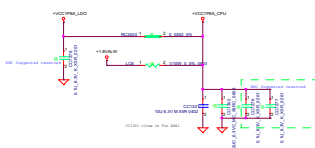
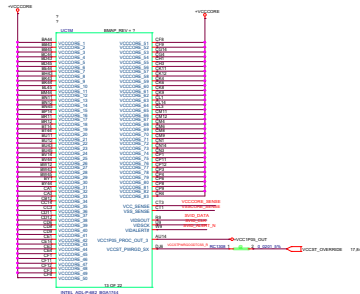


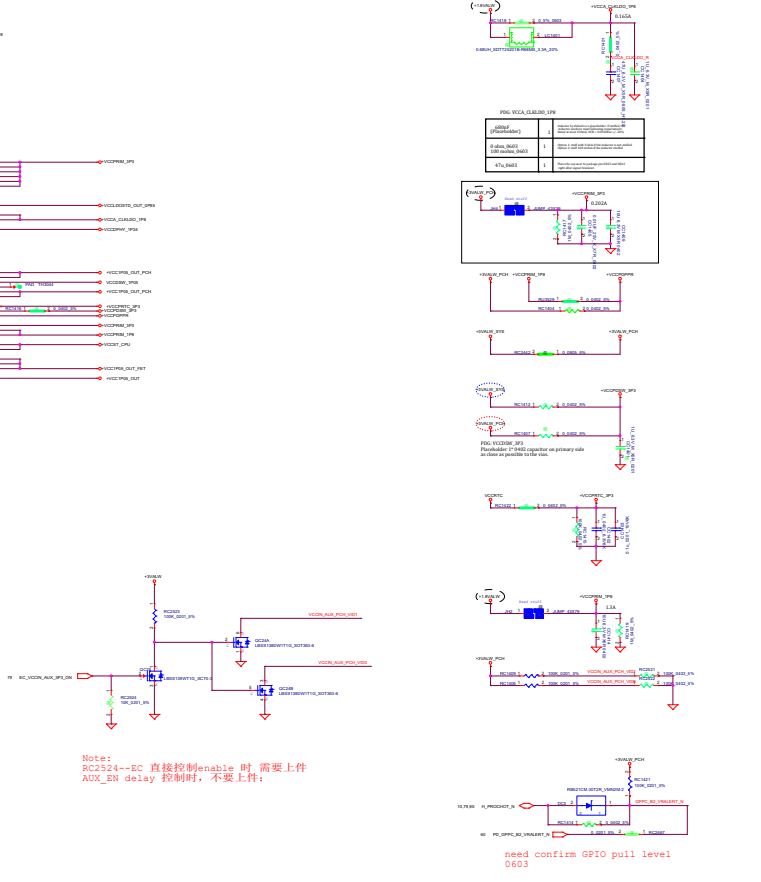
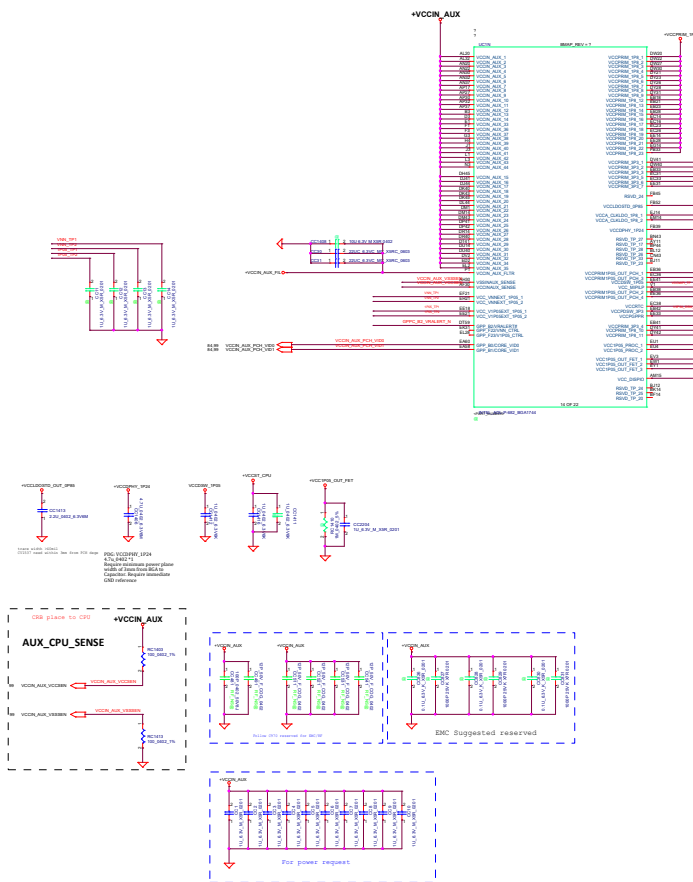


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A3	VSS 1 VSS 74	AL17	CD58	DC47	VSS 2VSS 369	ED58	F56	VSS 4VSS 5	M56
A17	VSS 2 VSS 75	AL22	CD59	DC54	VSS 2VSS 370	ED59	F59	VSS 4VSS 6	M57
A22	VSS 3 VSS 76	AL27	CD60	DC59	VSS 2VSS 371	ED60	F60	VSS 4VSS 7	M58
A27	VSS 4 VSS 77	AL32	CD61	DC64	VSS 2VSS 372	ED61	F61	VSS 4VSS 8	M59
A32	VSS 5 VSS 78	AL37	CD62	DC69	VSS 2VSS 373	ED62	F62	VSS 4VSS 9	M60
A37	VSS 6 VSS 79	AL42	CD63	DC74	VSS 2VSS 374	ED63	F63	VSS 4VSS 10	M61
A42	VSS 7 VSS 80	AL47	CD64	DC79	VSS 2VSS 375	ED64	F64	VSS 4VSS 11	M62
A47	VSS 8 VSS 81	AL52	CD65	DC84	VSS 2VSS 376	ED65	F65	VSS 4VSS 12	M63
A52	VSS 9 VSS 82	AL57	CD66	DC89	VSS 2VSS 377	ED66	F66	VSS 4VSS 13	M64
A57	VSS 10 VSS 83	AL62	CD67	DC94	VSS 2VSS 378	ED67	F67	VSS 4VSS 14	M65
A62	VSS 11 VSS 84	AL67	CD68	DC99	VSS 2VSS 379	ED68	F68	VSS 4VSS 15	M66
A67	VSS 12 VSS 85	AL72	CD69	DC04	VSS 2VSS 380	ED69	F69	VSS 4VSS 16	M67
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A77	VSS 14 VSS 87	AL82	CD71	DC14	VSS 2VSS 382	ED71	F71	VSS 4VSS 18	M69
A82	VSS 15 VSS 88	AL87	CD72	DC19	VSS 2VSS 383	ED72	F72	VSS 4VSS 19	M70
A87	VSS 16 VSS 89	AL92	CD73	DC24	VSS 2VSS 384	ED73	F73	VSS 4VSS 20	M71
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A17	VSS 22 VSS 95	AL22	CD79	DC54	VSS 2VSS 390	ED79	F79	VSS 4VSS 26	M77
A22	VSS 23 VSS 96	AL27	CD80	DC59	VSS 2VSS 391	ED80	F80	VSS 4VSS 27	M78
A27	VSS 24 VSS 97	AL32	CD81	DC64	VSS 2VSS 392	ED81	F81	VSS 4VSS 28	M79
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A62	VSS 31 VSS 104	AL67	CD88	DC99	VSS 2VSS 399	ED88	F88	VSS 4VSS 35	M86
A67	VSS 32 VSS 105	AL72	CD89	DC04	VSS 2VSS 400	ED89	F89	VSS 4VSS 36	M87
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A47	VSS 48 VSS 121	AL52	CD05	DC84	VSS 2VSS 416	ED05	F05	VSS 4VSS 52	M03
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A57	VSS 50 VSS 123	AL62	CD07	DC94	VSS 2VSS 418	ED07	F07	VSS 4VSS 54	M05
A62	VSS 51 VSS 124	AL67	CD08	DC99	VSS 2VSS 419	ED08	F08	VSS 4VSS 55	M06
A67	VSS 52 VSS 125	AL72	CD09	DC04	VSS 2VSS 420	ED09	F09	VSS 4VSS 56	M07
A72	VSS 53 VSS 126	AL77	CD10	DC09	VSS 2VSS 421	ED10	F10	VSS 4VSS 57	M08
A77	VSS 54 VSS 127	AL82	CD11	DC14	VSS 2VSS 422	ED11	F11	VSS 4VSS 58	M09
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A92	VSS 57 VSS 130	AL97	CD14	DC29	VSS 2VSS 425	ED14	F14	VSS 4VSS 61	M12
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A02	VSS 59 VSS 132	AL07	CD16	DC39	VSS 2VSS 427	ED16	F16	VSS 4VSS 63	M14
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A12	VSS 61 VSS 134	AL17	CD18	DC49	VSS 2VSS 429	ED18	F18	VSS 4VSS 65	M16
A17	VSS 62 VSS 135	AL22	CD19	DC54	VSS 2VSS 430	ED19	F19	VSS 4VSS 66	M17
A22	VSS 63 VSS 136	AL27	CD20	DC59	VSS 2VSS 431	ED20	F20	VSS 4VSS 67	M18
A27	VSS 64 VSS 137	AL32	CD21	DC64	VSS 2VSS 432	ED21	F21	VSS 4VSS 68	M19
A32	VSS 65 VSS 138	AL37	CD22	DC69	VSS 2VSS 433	ED22	F22	VSS 4VSS 69	M20
A37	VSS 66 VSS 139	AL42	CD23	DC74	VSS 2VSS 434	ED23	F23	VSS 4VSS 70	M21
A42	VSS 67 VSS 140	AL47	CD24	DC79	VSS 2VSS 435	ED24	F24	VSS 4VSS 71	M22
A47	VSS 68 VSS 141	AL52	CD25	DC84	VSS 2VSS 436	ED25	F25	VSS 4VSS 72	M23
A52	VSS 69 VSS 142	AL57	CD26	DC89	VSS 2VSS 437	ED26	F26	VSS 4VSS 73	M24
A57	VSS 70 VSS 143	AL62	CD27	DC94	VSS 2VSS 438	ED27	F27	VSS 4VSS 74	M25
A62	VSS 71 VSS 144	AL67	CD28	DC99	VSS 2VSS 439	ED28	F28	VSS 4VSS 75	M26
A67	VSS 72 VSS 145	AL72	CD29	DC04	VSS 2VSS 440	ED29	F29	VSS 4VSS 76	M27
A72	VSS 73 VSS 146	AL77	CD30	DC09	VSS 2VSS 441	ED30	F30	VSS 4VSS 77	M28
A77	VSS 74 VSS 147	AL82	CD31	DC14	VSS 2VSS 442	ED31	F31	VSS 4VSS 78	M29
A82	VSS 75 VSS 148	AL87	CD32	DC19	VSS 2VSS 443	ED32	F32	VSS 4VSS 79	M30



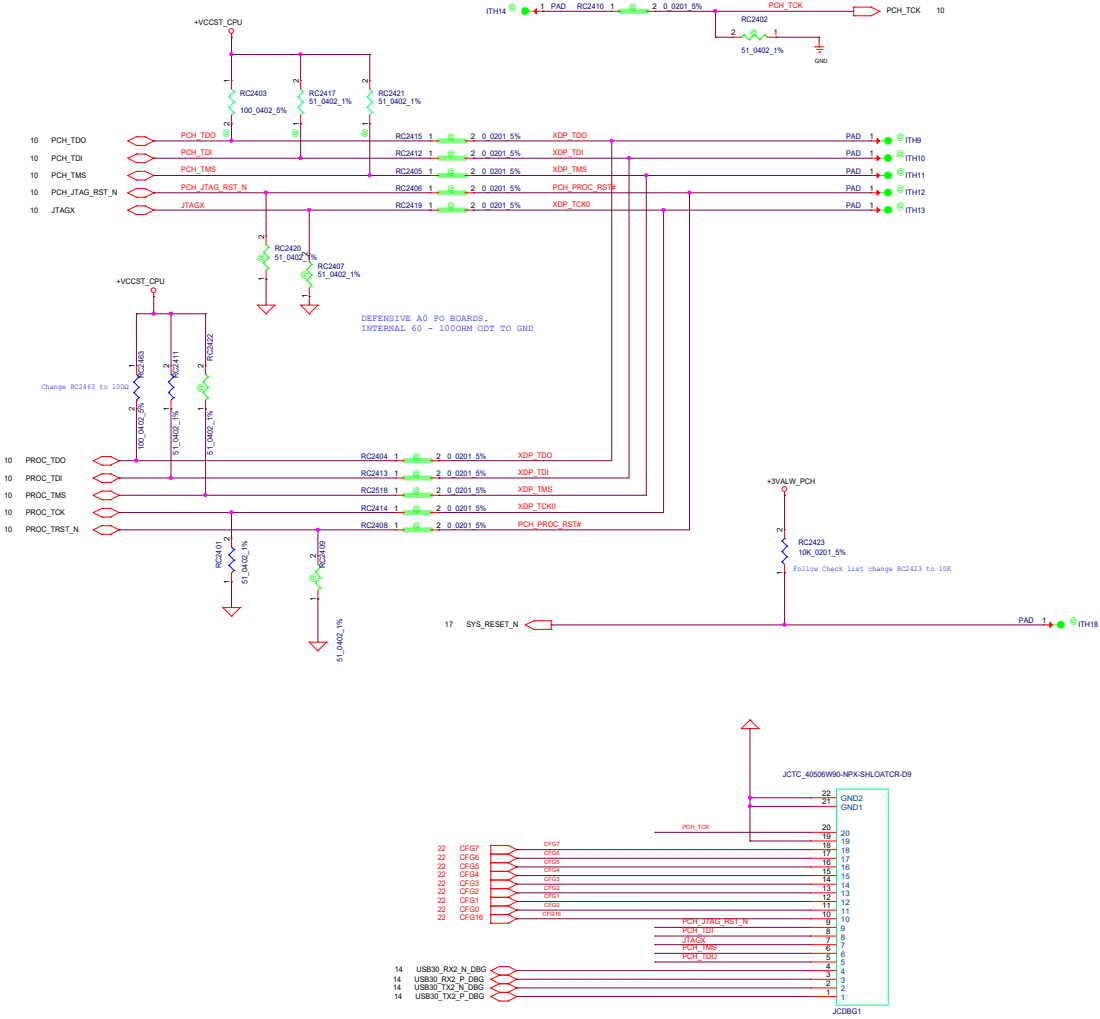
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TABLE : CPU ITP DEBUG REPORT

	No use	Individual Port	DCI 2.0 w/o connector
R591	NO ASM	NO ASM	ASM
R593	NO ASM	NO ASM	ASM
R594	NO ASM	NO ASM	ASM
R595	NO ASM	NO ASM	ASM
R596	NO ASM	NO ASM	ASM
R657	NO ASM	NO ASM	ASM
R658	NO ASM	NO ASM	ASM
R102	NO ASM	ASM	NO ASM
R597	NO ASM	ASM	NO ASM
R9907	NO ASM	ASM	ASM
JXDP1	NO ASM	ASM	NO ASM
C70	NO ASM	ASM	NO ASM
R96	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9909	NO ASM	ASM	ASM
R9910	NO ASM	ASM	ASM
R9916	NO ASM	ASM	ASM
R99	NO ASM	ASM	ASM
R9912	NO ASM	ASM	ASM
R9934	NO ASM	ASM	ASM
R9930	NO ASM	ASM	ASM
R9931	NO ASM	ASM	ASM
R9932	NO ASM	ASM	ASM
R9933	NO ASM	ASM	ASM

TABLE : PCH ITP DEBUG REPORT

	No use	Individual Port	DCI 2.0 w/o connector
R93	NO ASM	ASM	NO ASM
JXDP1	NO ASM	ASM	NO ASM
R9917	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9908	NO ASM	ASM	NO ASM
R9911	NO ASM	ASM	NO ASM
R9913	NO ASM	ASM	NO ASM
R9915	NO ASM	ASM	NO ASM





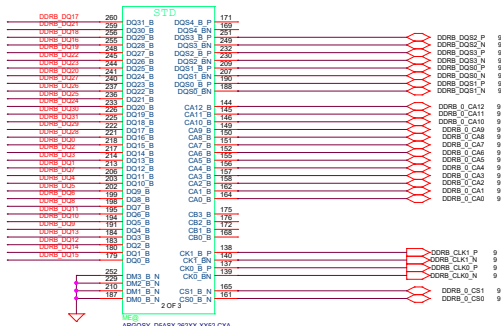




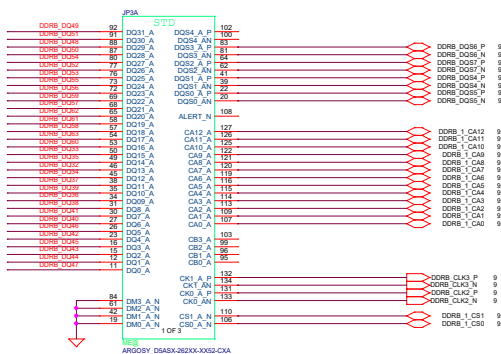
9 DDRB\_DQ0\_63 DDRB\_DQ63\_63

JF8B

10K 20.0K 001



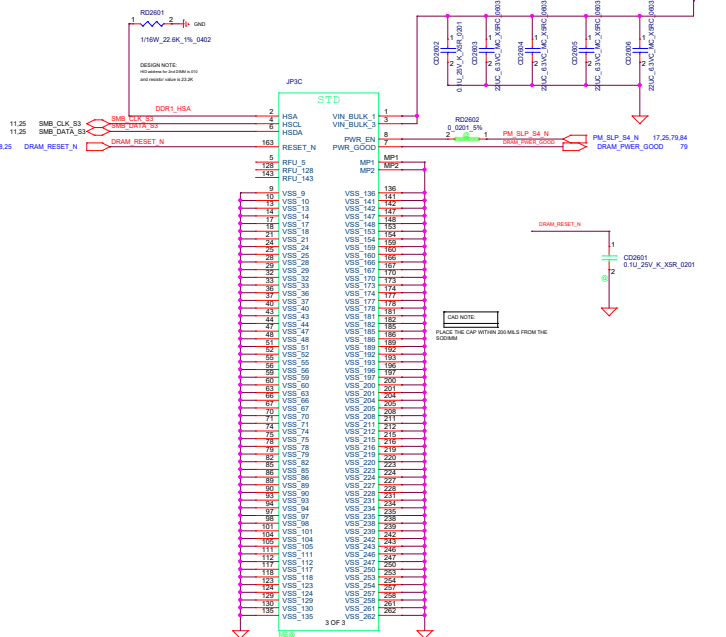
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ARGOSY\_DS65X-262XX-KX32-CXA

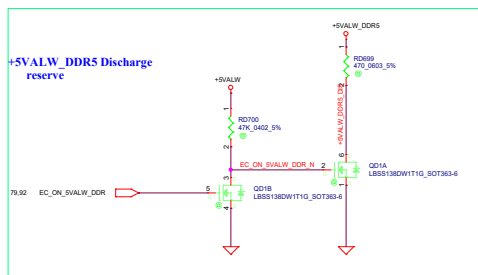
DESIGN NOTE

pin 541 542(1-1) 1

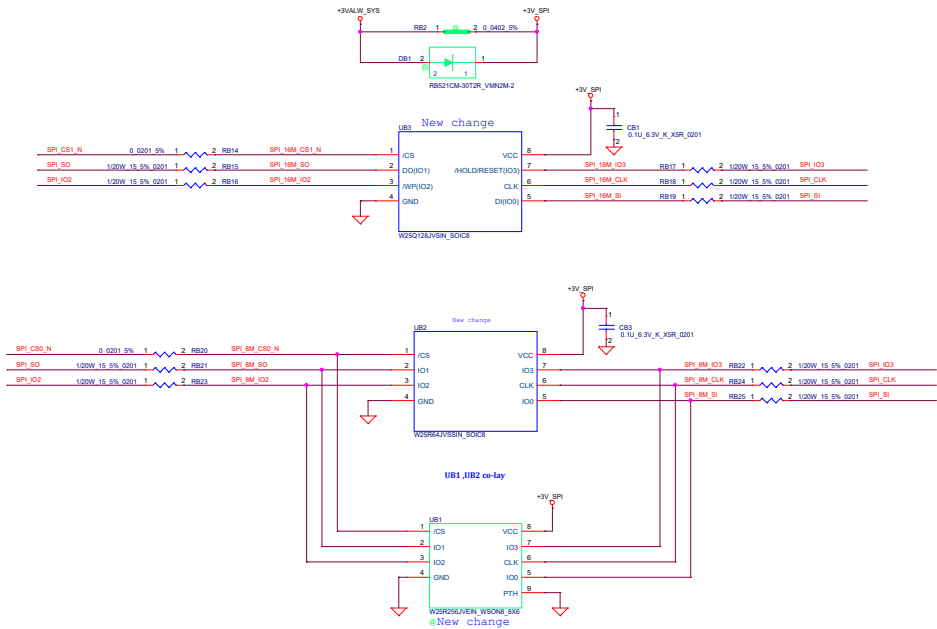
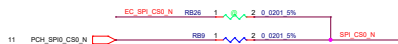
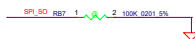
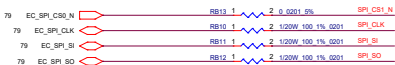
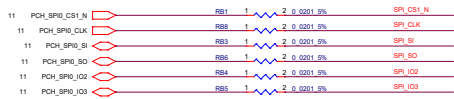


BPAGE DRAWING

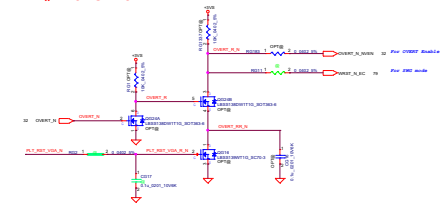
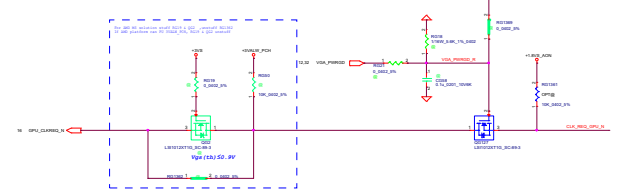
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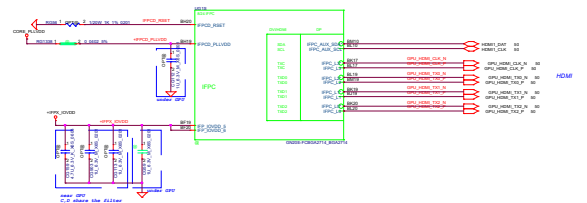
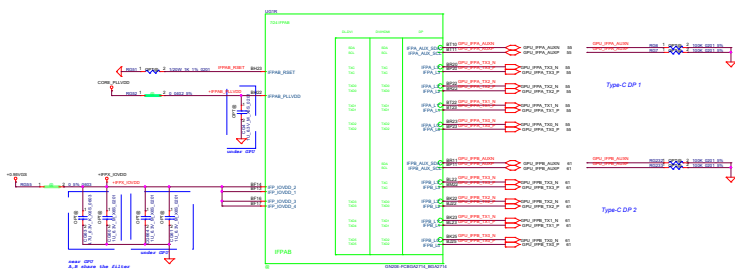
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Size		Document Number		Rev	
C		YXO ORS		1	
Date		Monday, November 29, 2021		[Sheet 26 of 110]	



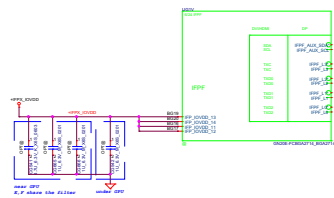
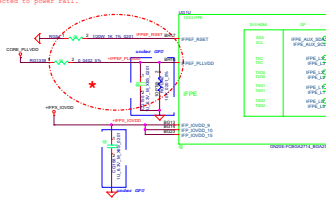
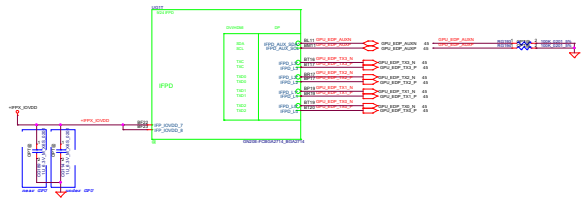
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Size		C		Document Number		Rev
				SPI ROM/TPM		A0
Date		Monday, November 25, 2021		Information		27 of 116

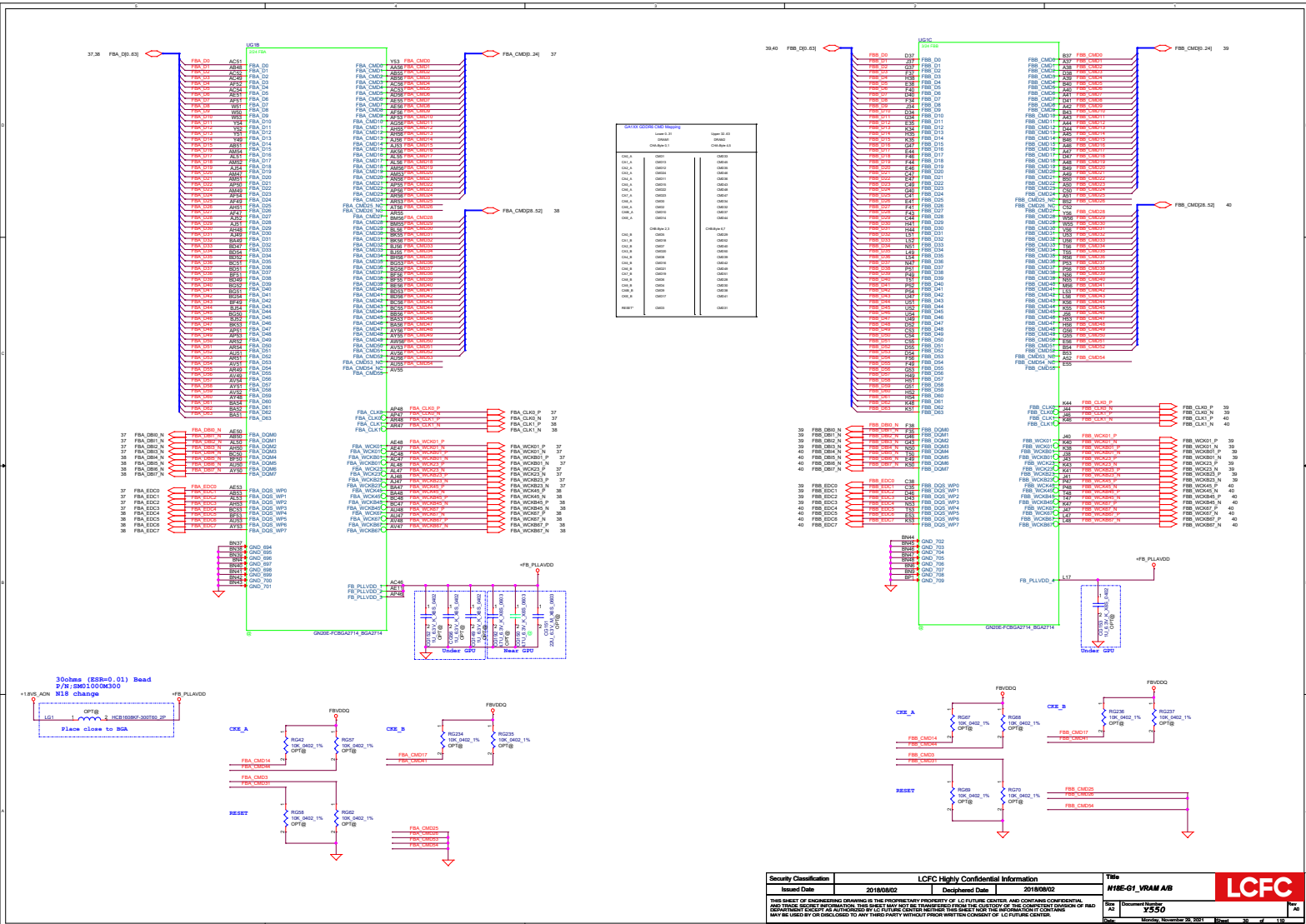


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Doc No.	Document Number		Value	Rev
			Y550	01
Date: Monday, November 05, 2024 Status: Not in use				



1. If an IFF link is unused, the main and AUX links, IFFay\_AUX2 can be left unconnected, and IFFay\_AUX1 should be tied to GND.  
 2. IFF\_AUX2 rail can be left unconnected if no IFF link is used. If any IFF is used, all IFF\_AUX2 rails must be connected to power rail.

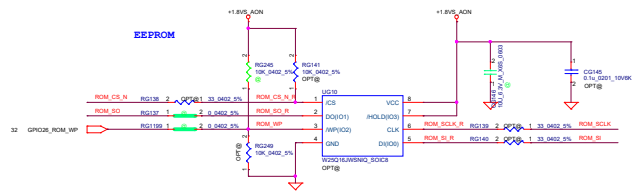
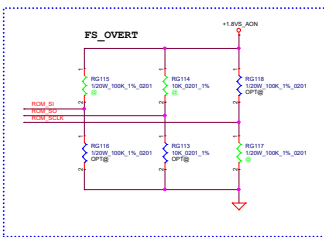
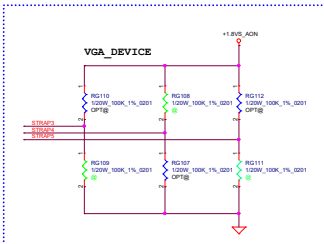
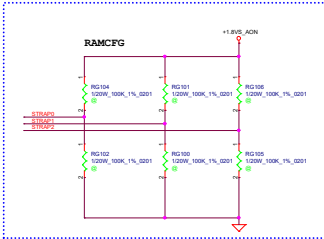
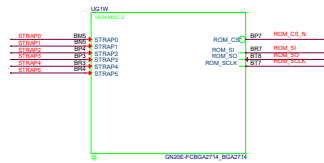












GPU VRAM	FB Memory (GDDR6)	RAMCFG[2:0]	STRAP0	STRAP1	STRAP2
GN20x-E7	Samsung 8Gb	K42803258C-BC14	0 (0x0000)	L	L
	Samsung 16Gb	K42AF3258M-BC 14	9 (0x0009)	L	M

GPU VRAM	FB Memory (GDDR6)	RAMCFG[2:0]	STRAP0	STRAP1	STRAP2
GN20x-E5	Samsung 8Gb	K42803258C-BC14	0 (0x0000)	L	L
GN20x-E3	Microon 8Gb	MT61K250K32JE-14:1A	1 (0x0001)	H	L
	Bylinx 8Gb	H56CB824LR-82C	2 (0x0002)	L	R

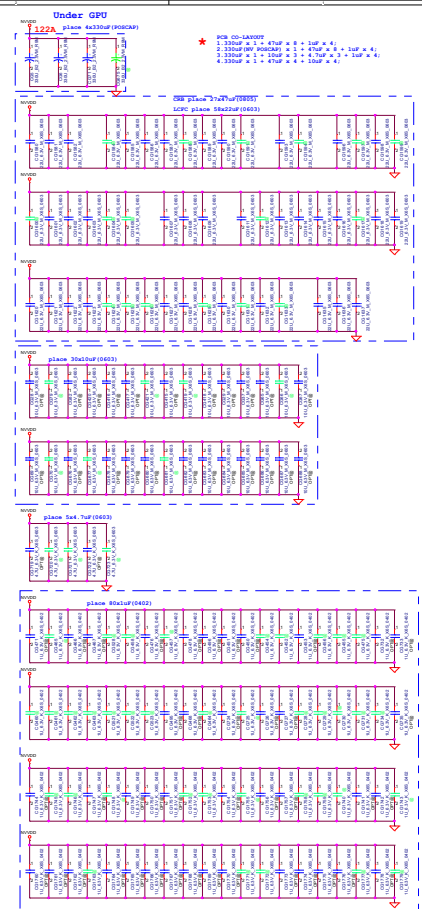
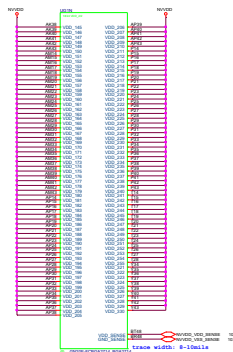
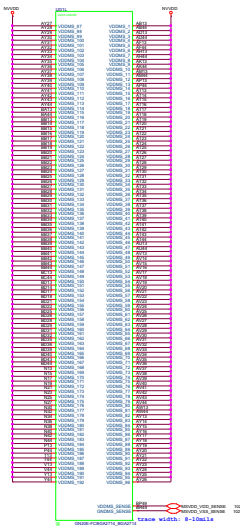
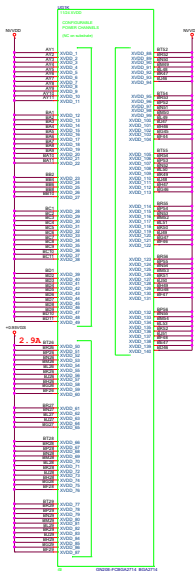
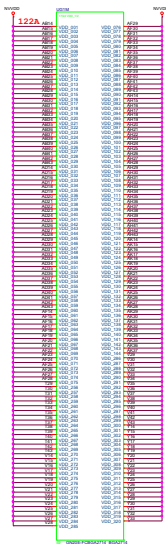
  

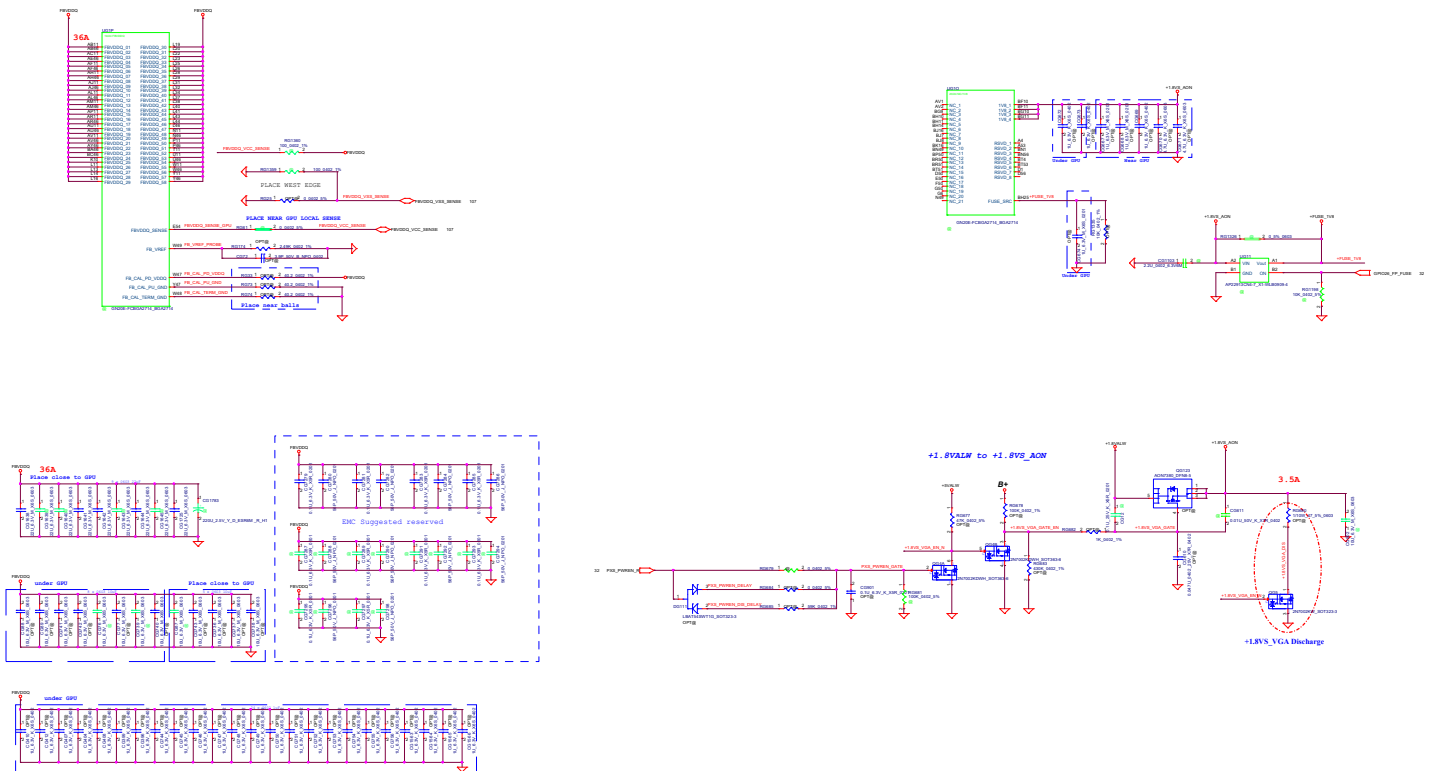
GPU VRAM	FB Memory (GDDR6)	RAMCFG[2:0]	STRAP0	STRAP1	STRAP2
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GN20x-E6	Samsung 16Gb	K42AF3258M-BC16	6 (0x0006)	L	R
	Bylinx 8Gb	H56G32C94DX005	5 (0x0005)	H	L

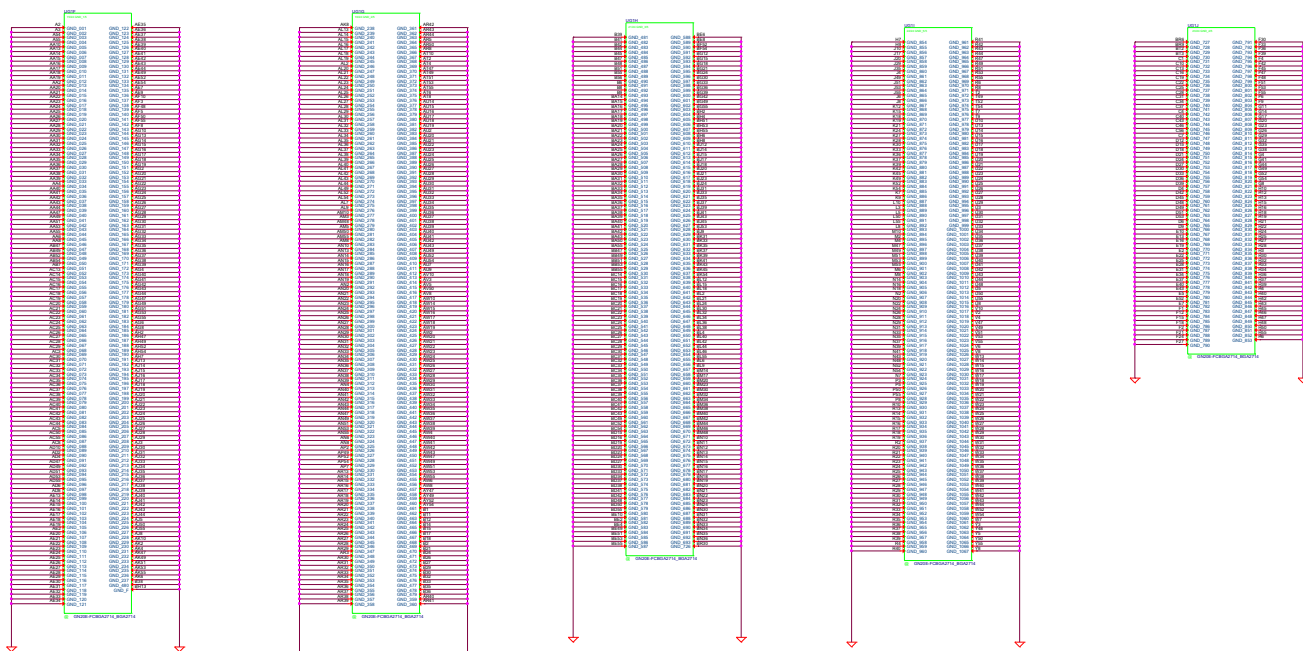
VGA_DEVICE E3E5E7					
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG
H	L	H	0	1	0

1:SMB\_ALT\_ADDR ENABLE  
0:SMB\_ALT\_ADDR DISABLE  
1:DEVID\_SEL REBRAND  
0:DEVID\_SEL ORIGINAL  
1:PCIE\_CFG LOW POWER  
0:PCIE\_CFG HIGH POWER  
1:VGA\_DEVICE ENABLE  
0:VGA\_DEVICE DISABLE

GPU	ROM_SO	ROM_SI	ROM_SCLK	FS_OVERT
GN20x	L	L	H	ENABLE

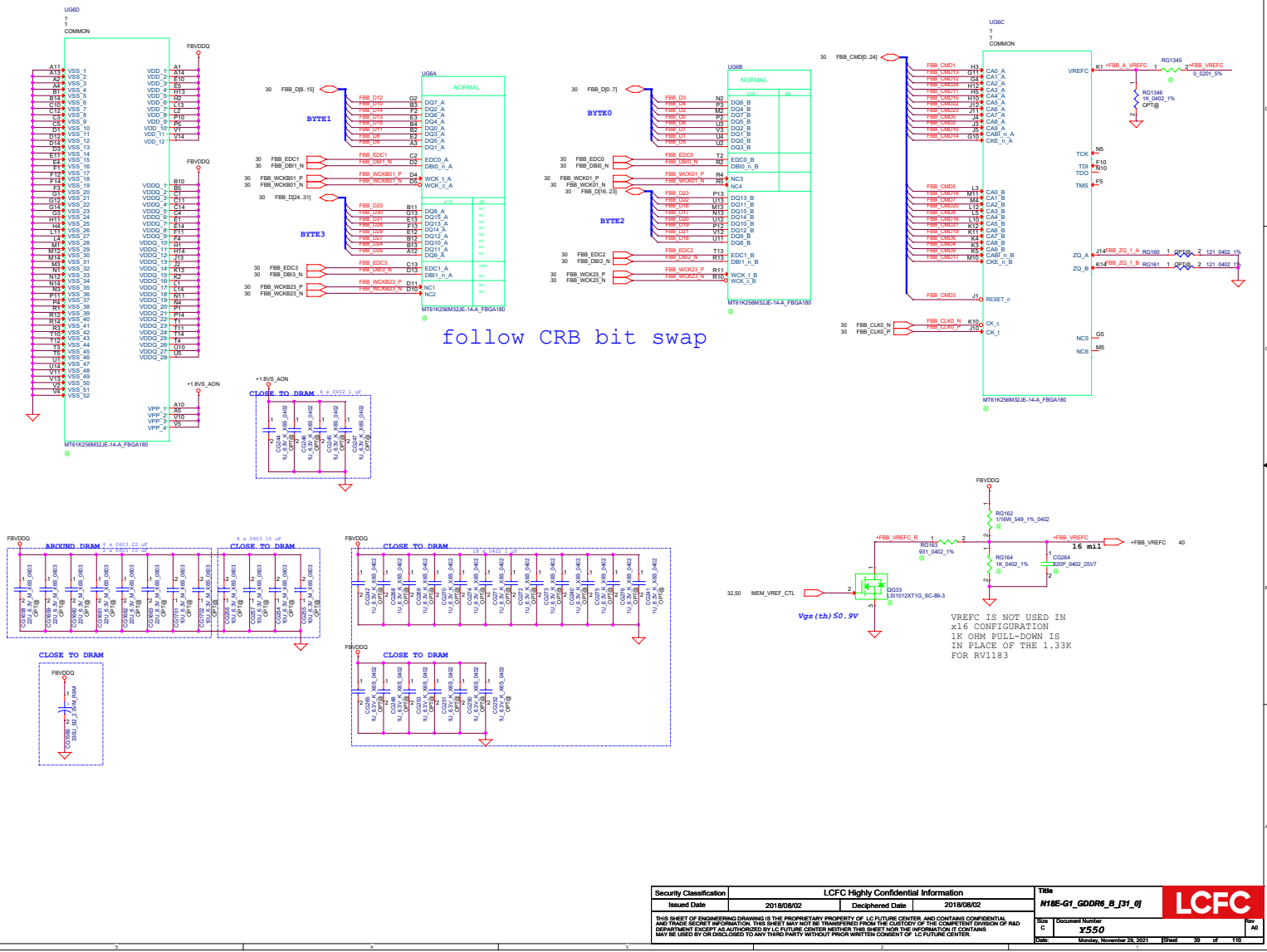








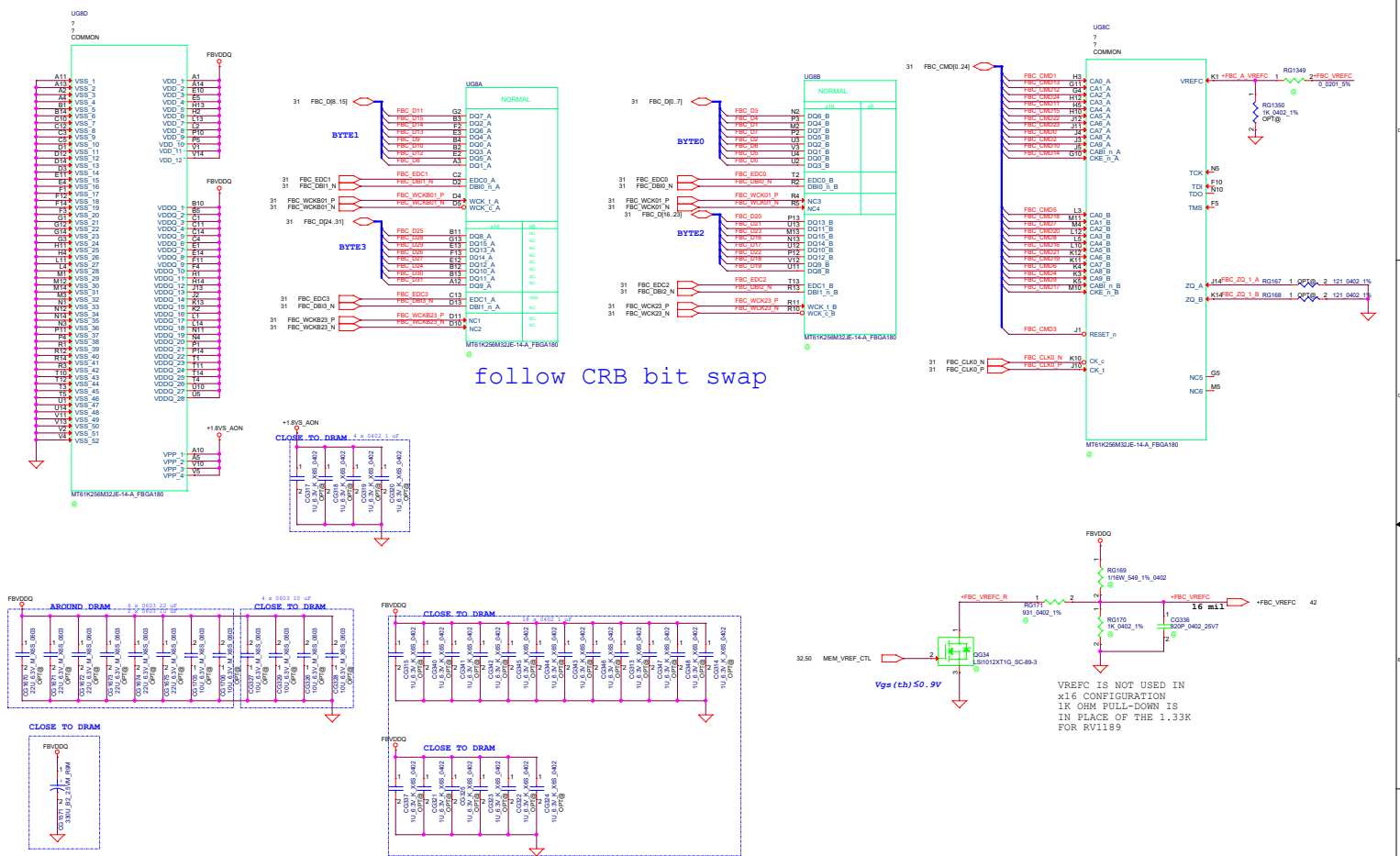


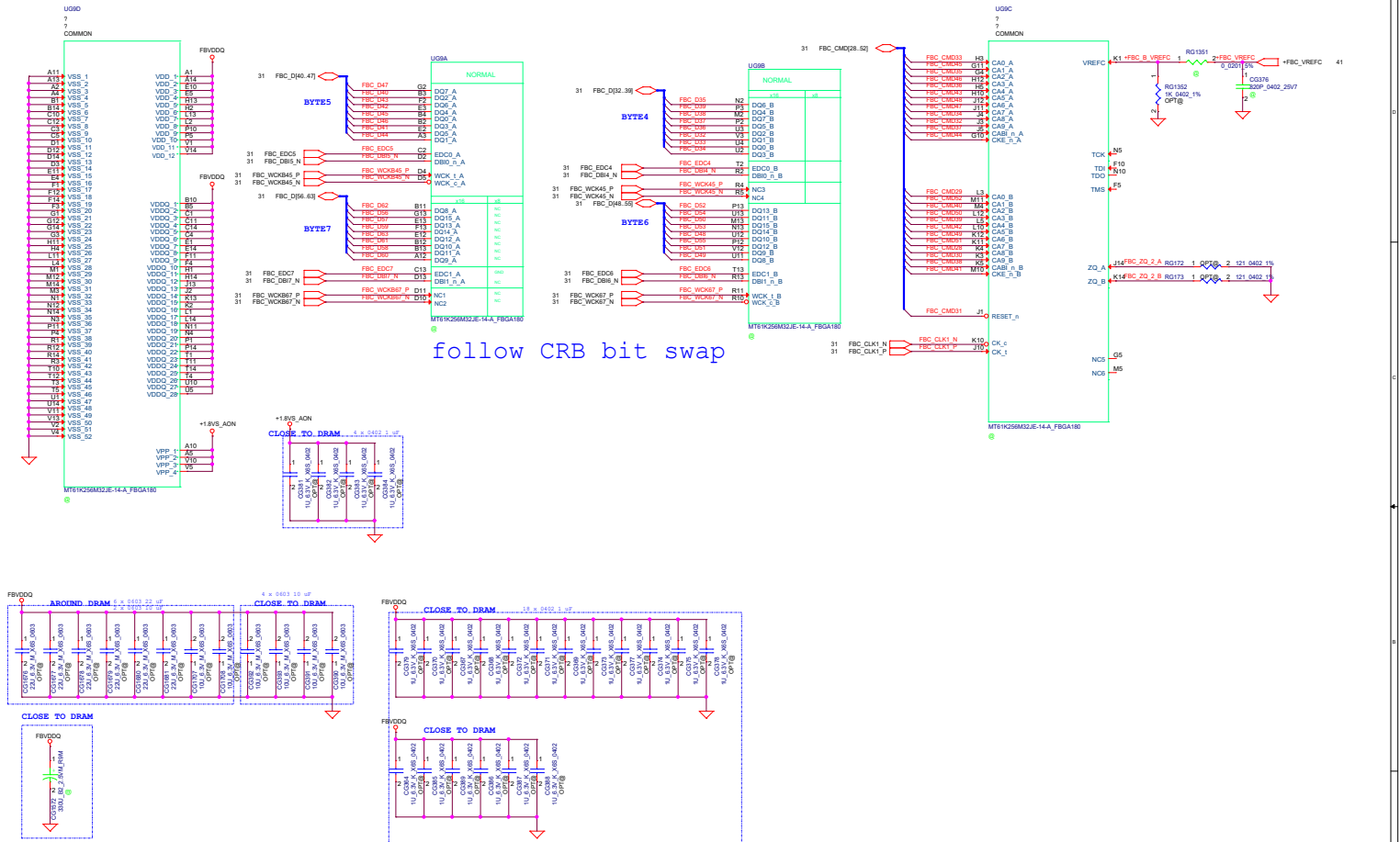


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				Doc	Y550
				Ver	1.0



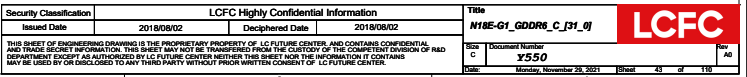


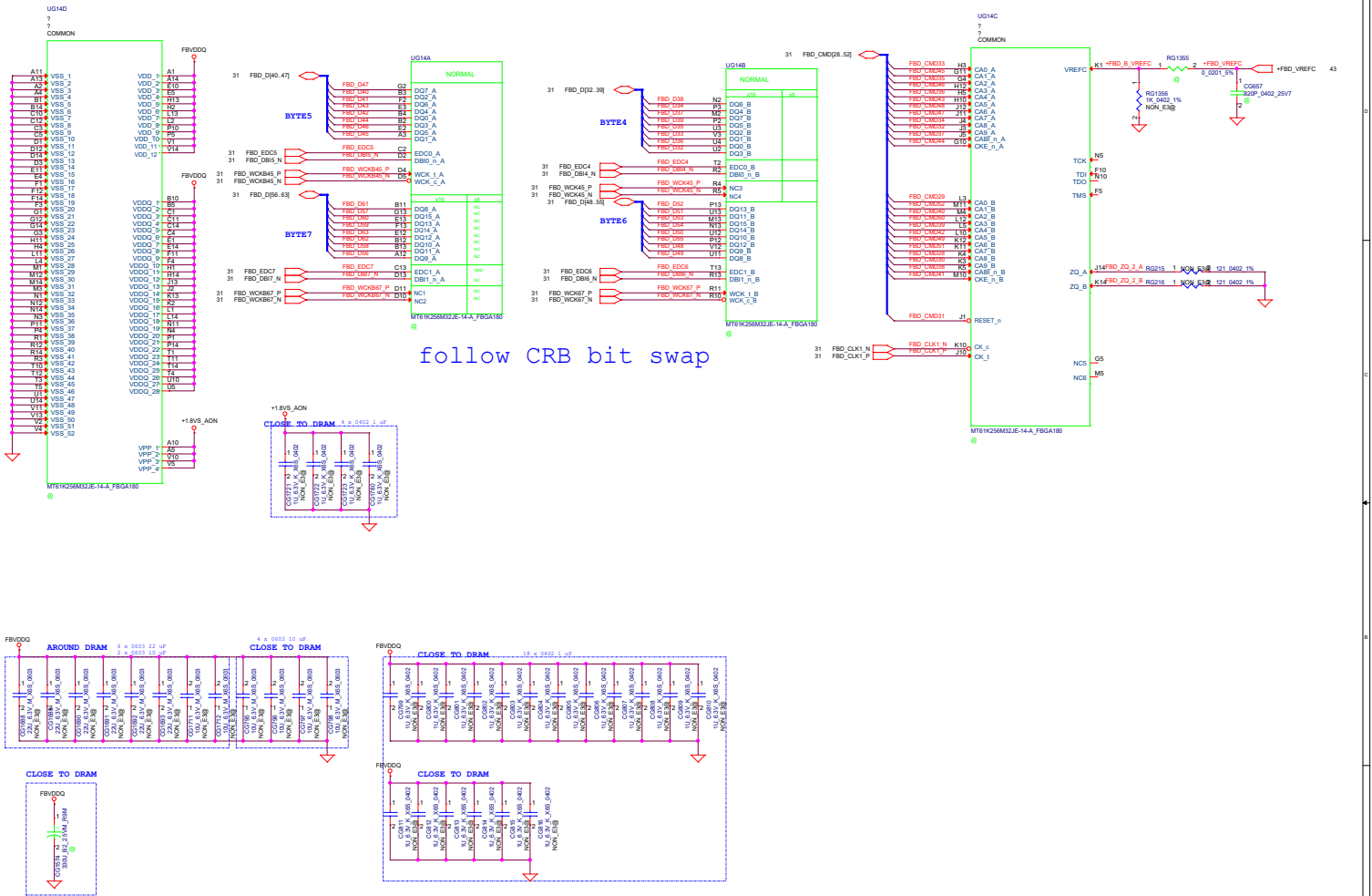




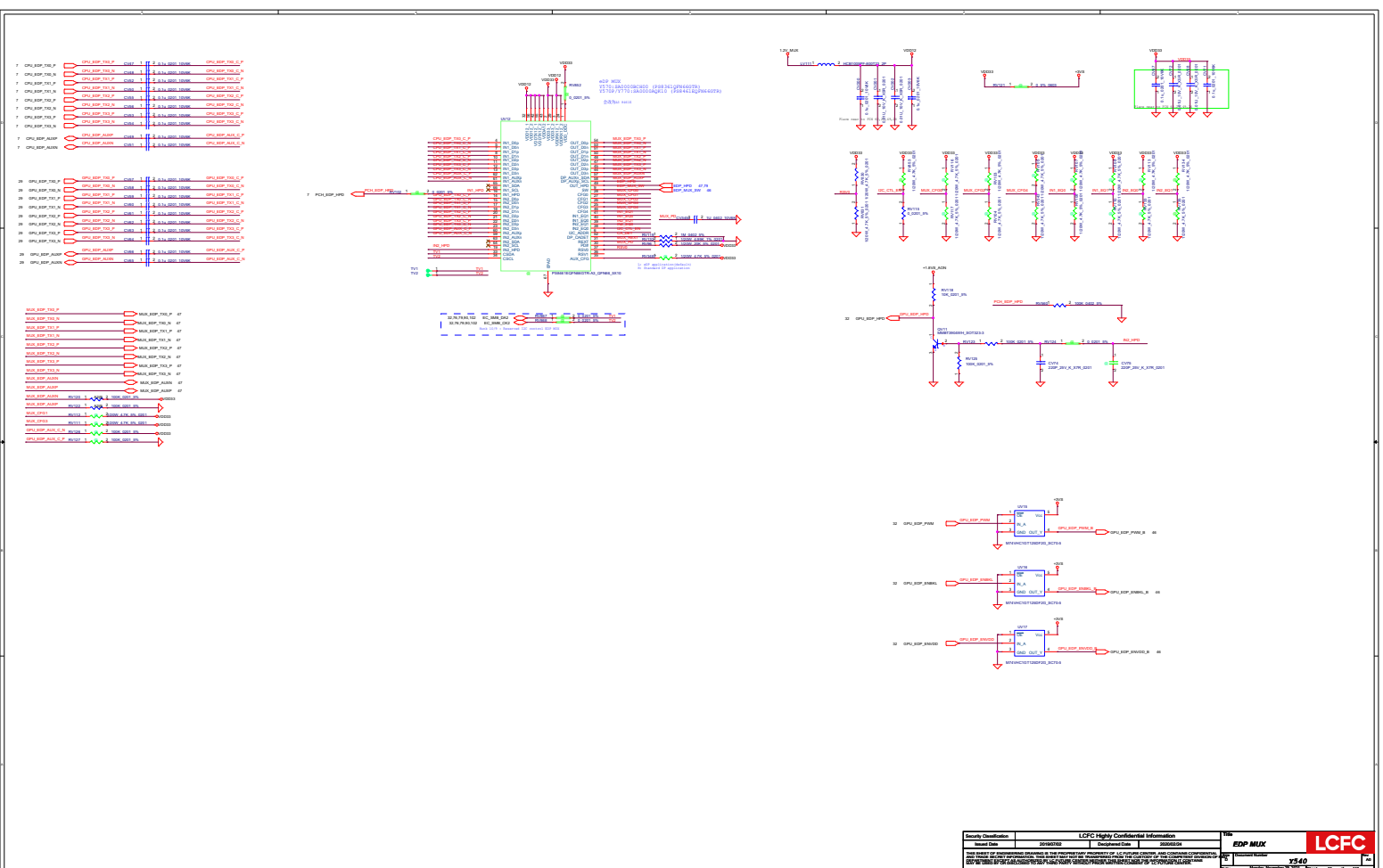
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				Doc	Y550
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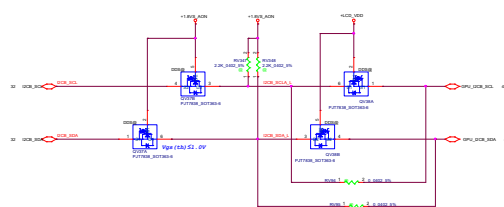
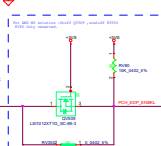
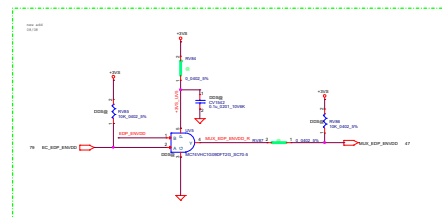
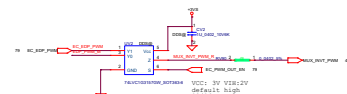
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				Rev	A0





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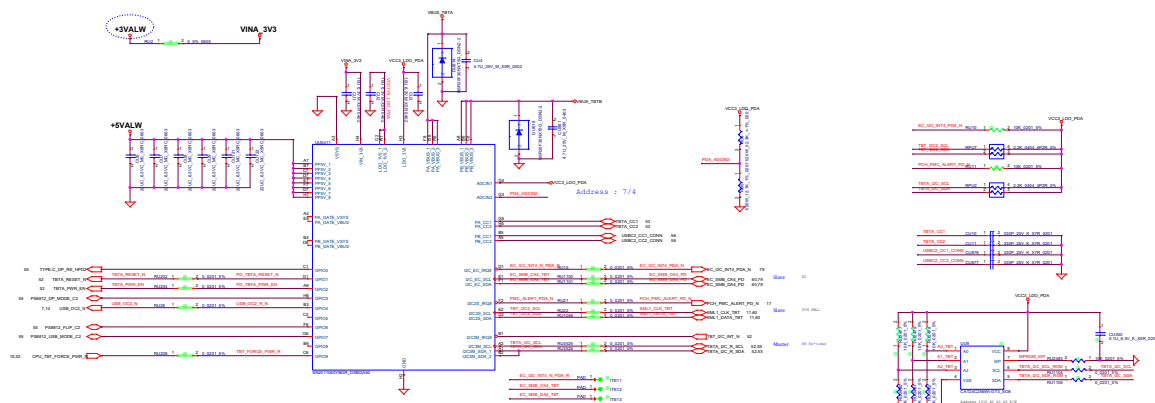



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Date:					Monday, November 29, 2021										Sheet					49 of 110					
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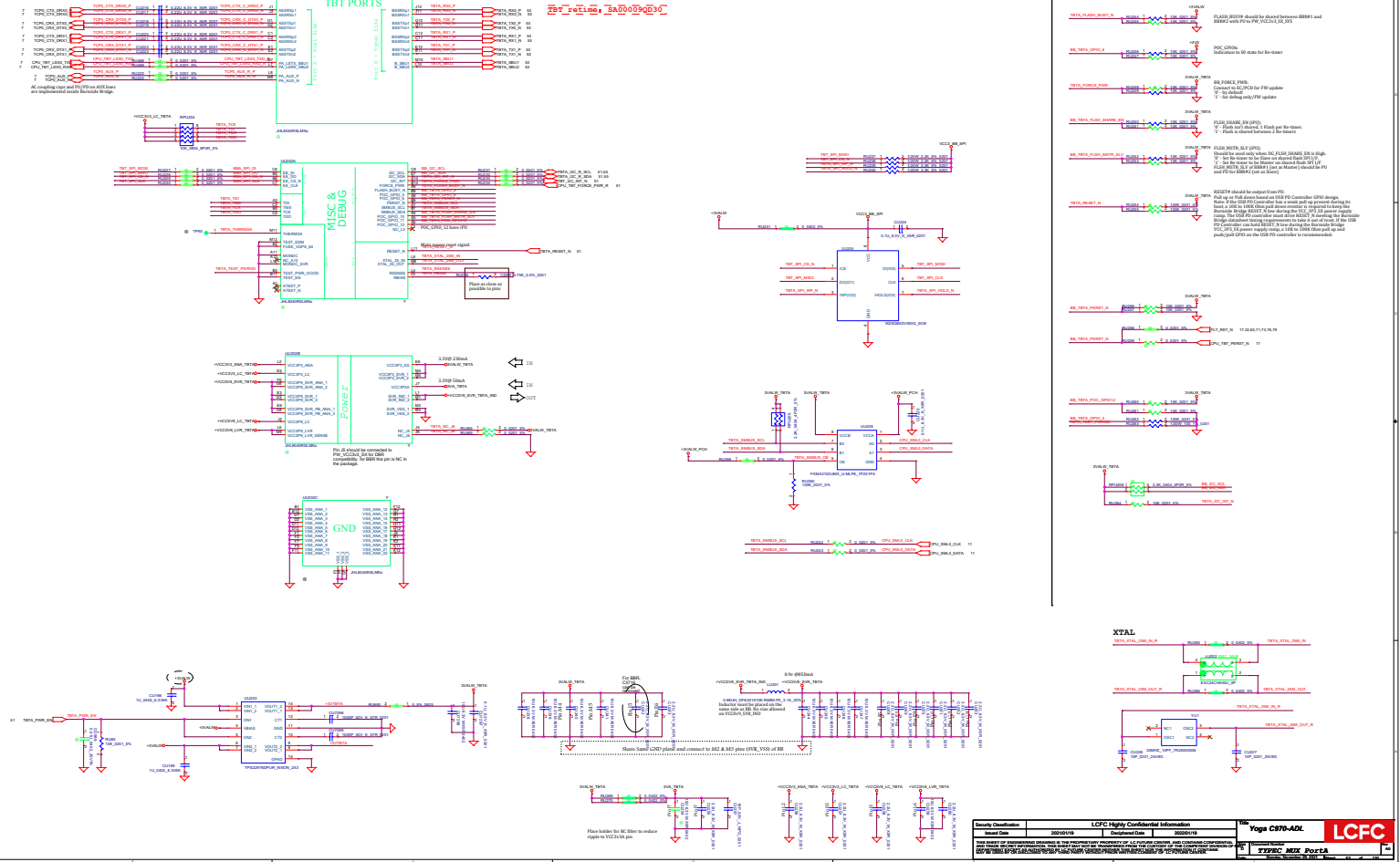


TBT portA/rear side

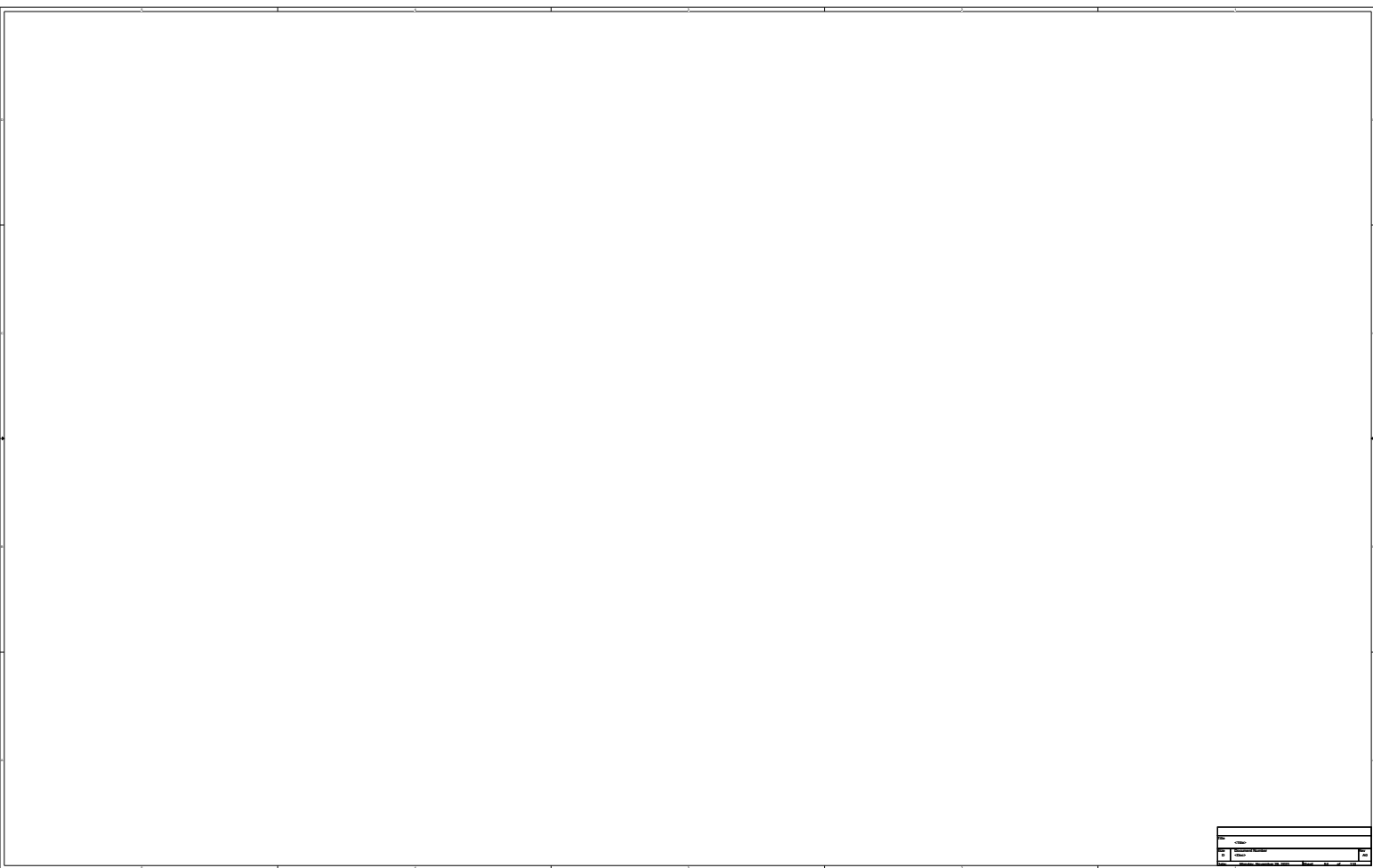


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			Account Number	TFPC Controller PortA	

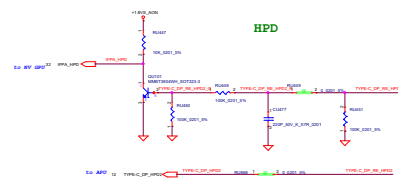
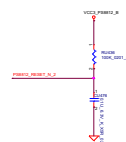
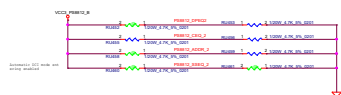
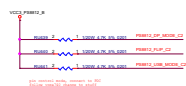
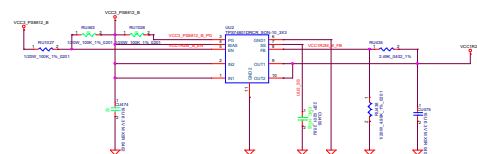
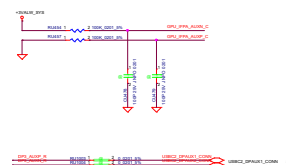
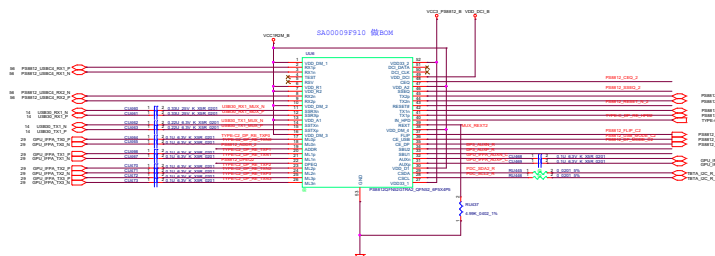
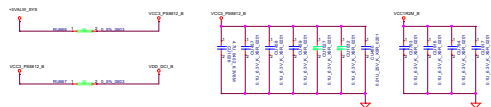
Burnside Bridge Re-Timer

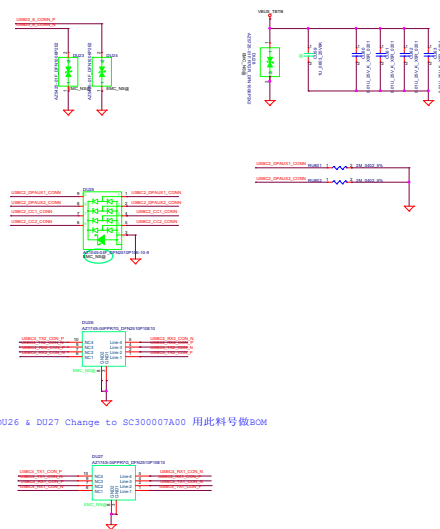
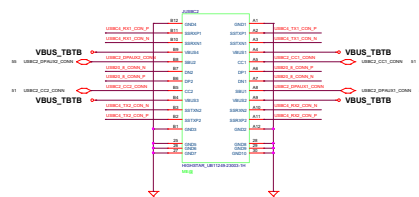
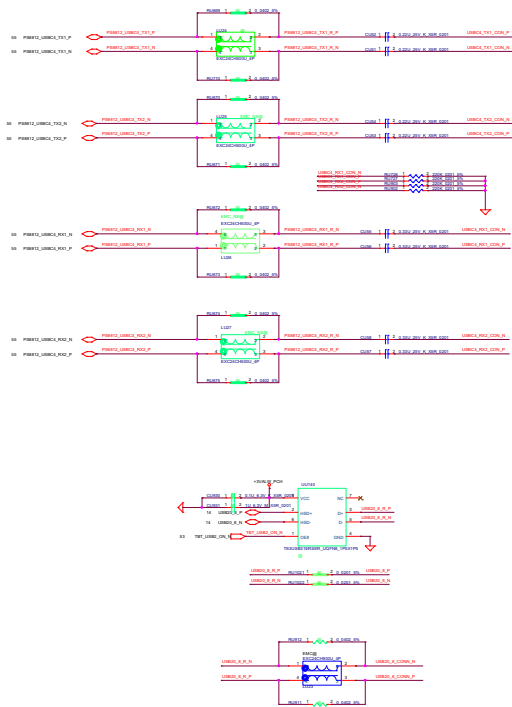






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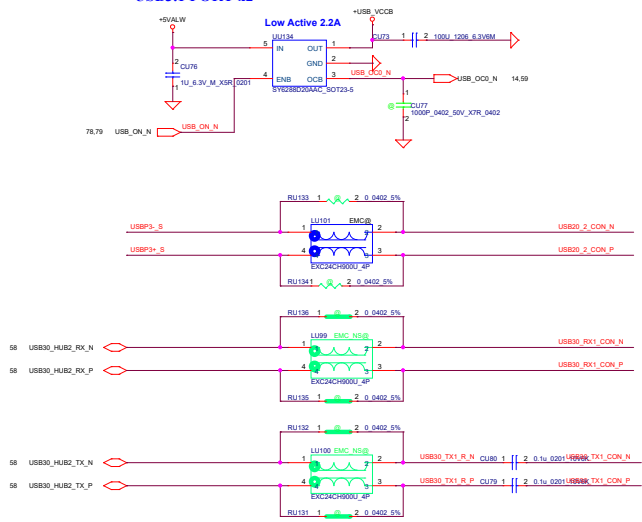




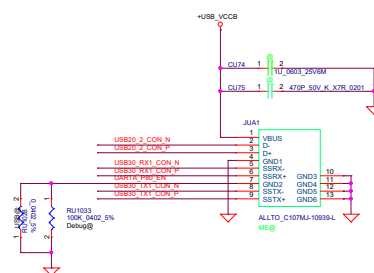
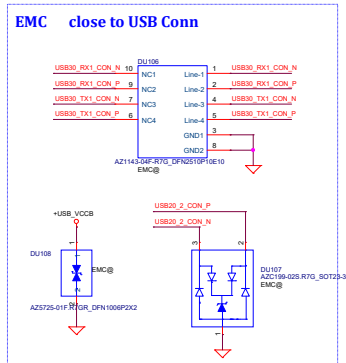
D026 & D027 Change to SC300007A00 用此料号做BOM



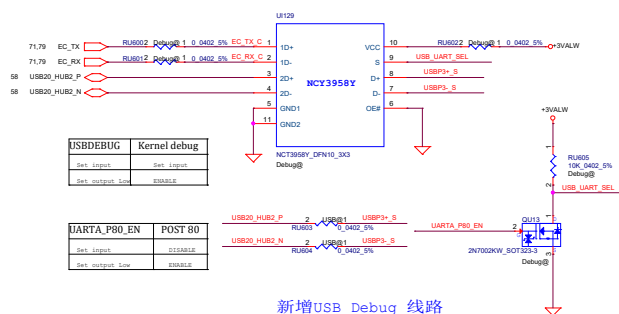
**USB3.1 PORT x2**



EMC close to USB Conn



### For USB Debug Function







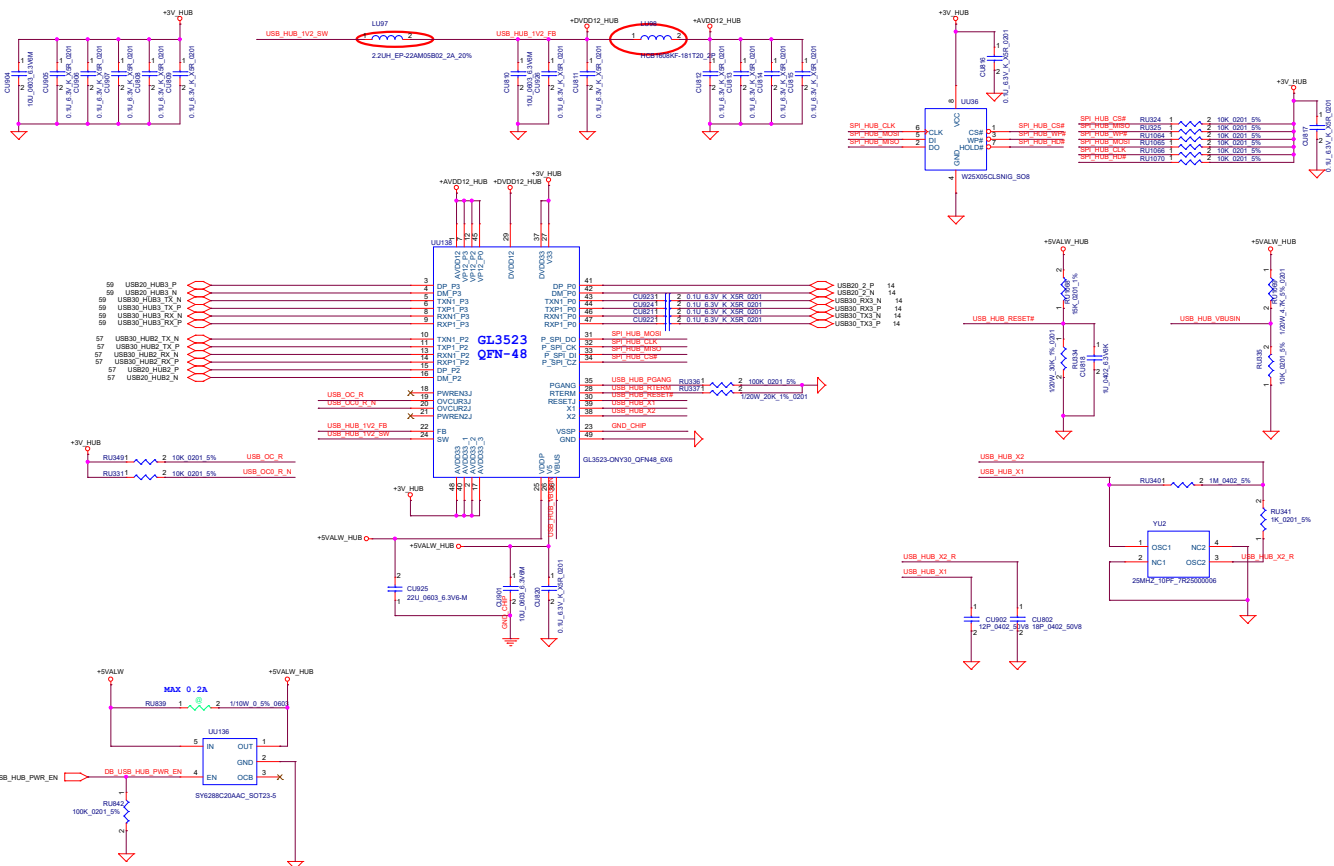
USBDEBUG	Kernel debug
Set input	Set input
Get output low	ENABLE

UART <sub>m</sub> P80 <sub>m</sub> EN	POST 80
Set input	DISABLE
Set output Low	ENABLE

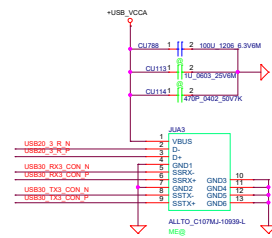
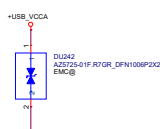
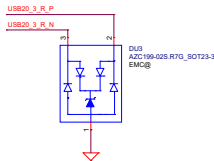
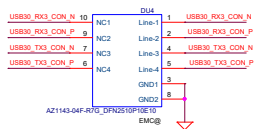
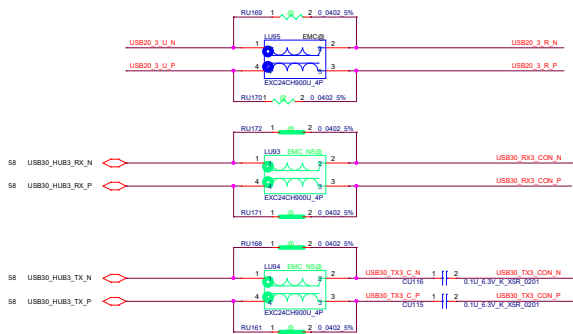
OE#	S	FUNCTION
H	X	DISABLE
L	L	D(4/-) to 1D(4/-)
L	H	D(4/+ ) to 2D(4/+)

## 新增USB Debug 线路

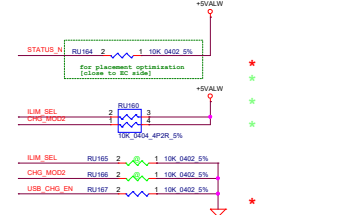
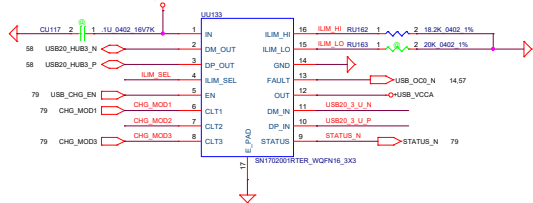
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Sheet		Document Number		y550			
Date		Monday, November 26, 2021		11:00			



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Rev C		Document Number		y550		Rev A0	
Date		Monday, November 28, 2017		Sheet		68 of 115	

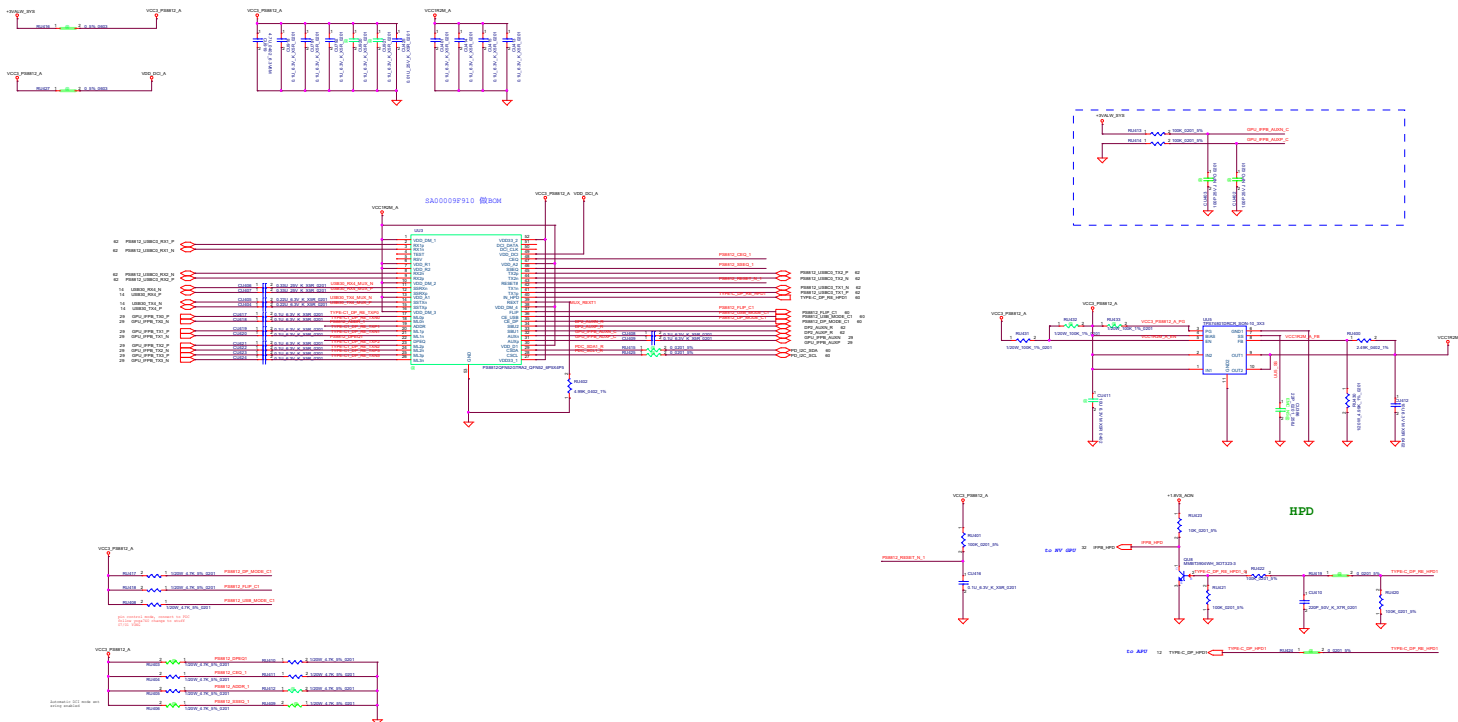


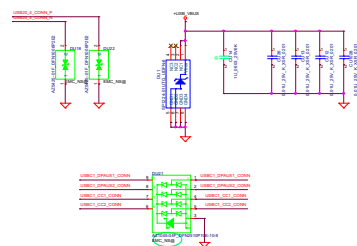
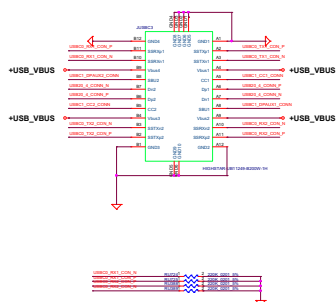
### USB charger 2.5A



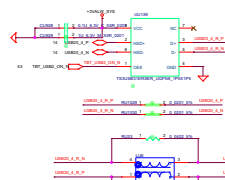
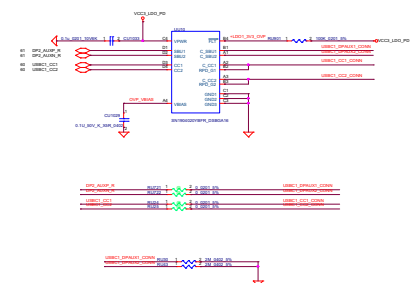
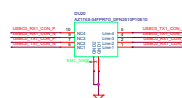
CLT1	CLT2	CLT3	ILM_SEL	MOD
0	0	0	X	DCR OUT held low
1	1	1	1	CDP Data Connected and Port Power Mgt. Function Active
1	1	1	0	SDP2 Data Connected
1	1	0	X	SDP1 Data Connected
0	1	0	X	SDP1 Data Connected
1	0	0	X	DCP_Short Device Forced to stay in DCP BC 1.2 charging mode
1	0	1	X	DCP_Divider Device Forced to stay in DCP Divider 1 Charging Mode
0	1	1	X	DCP_Auto Data Disconnected and Port Power Mgt. Function Active
0	0	1	X	DCP_Auto Data Disconnected and Power Wake Function Active



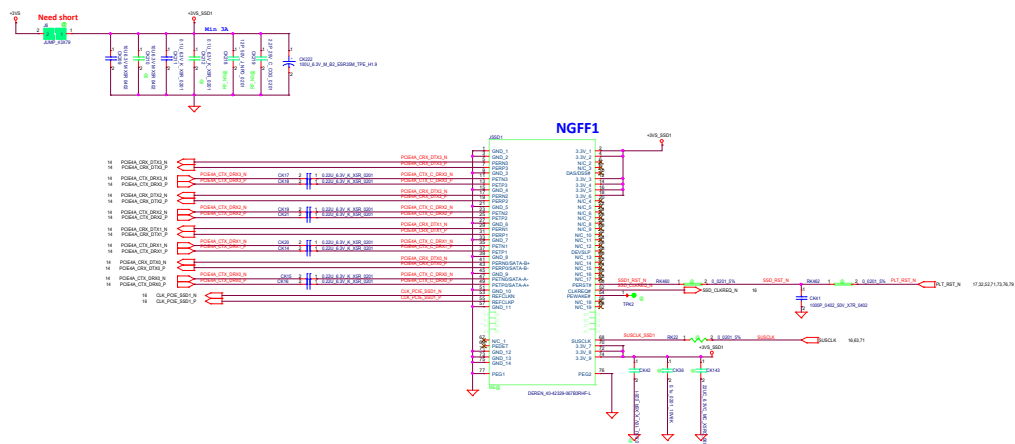




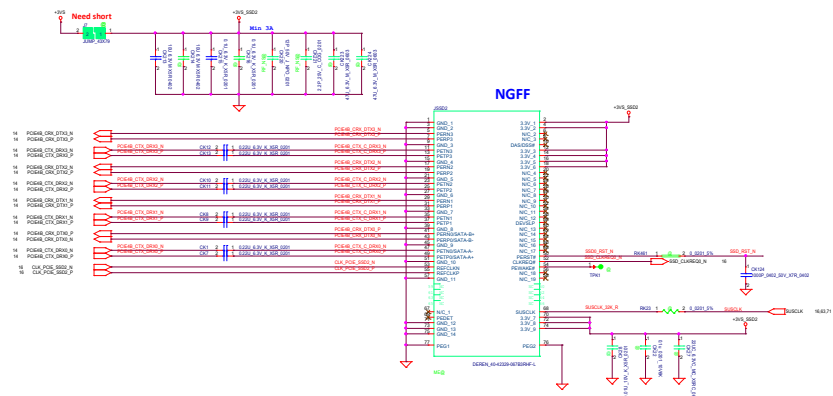
D019 & D020 Change to SC300007A00 用此料号做BCM



## M.2 SSD(PCIE GEN4 from CPU)



## M.2 SSD(SATA/PCIE Gen3 from PCH)

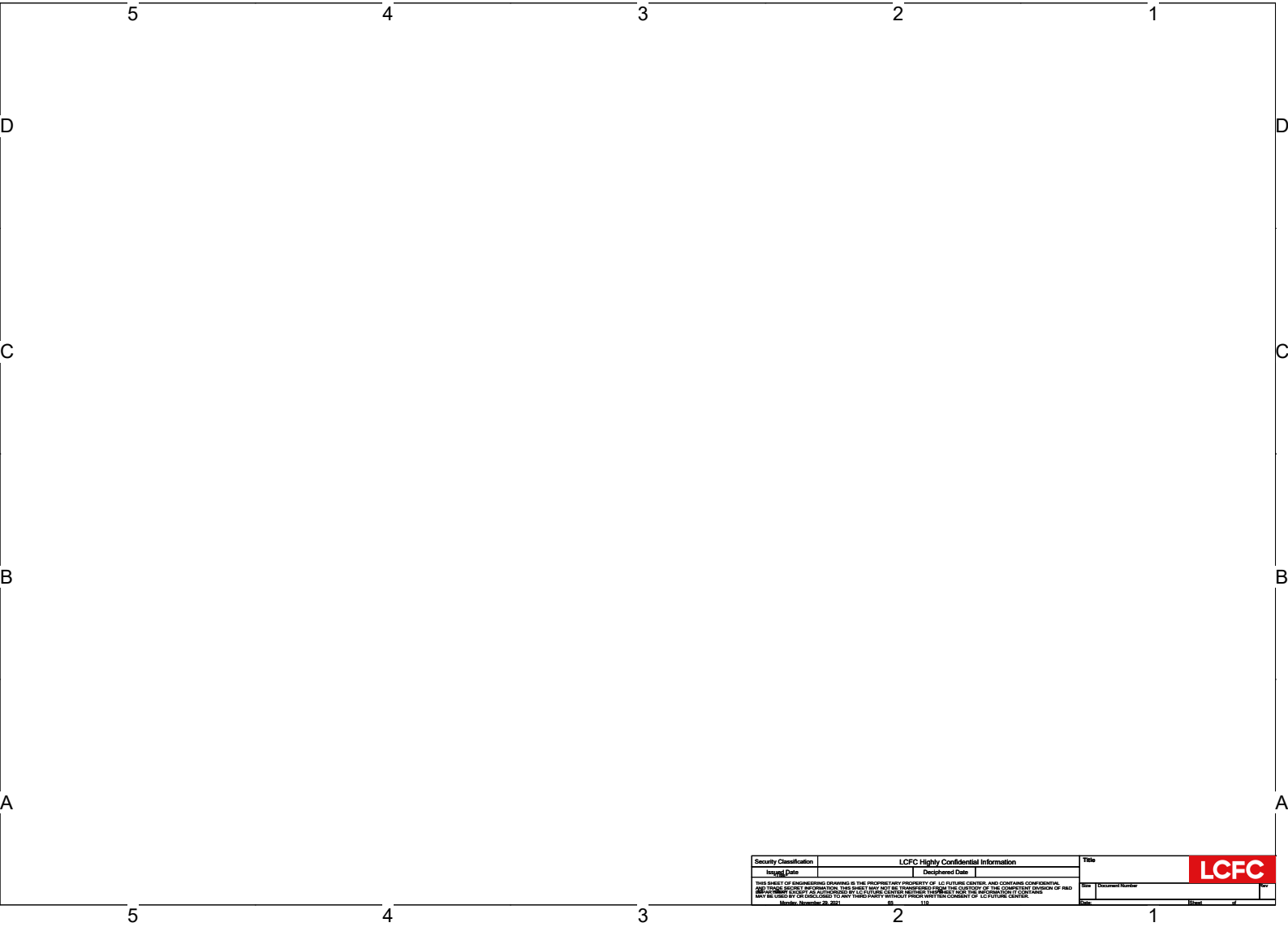


Delete USB3.0 Reapter Remove to DB board

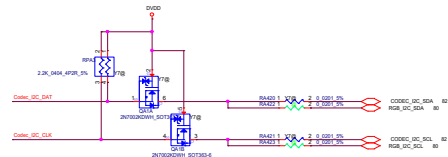
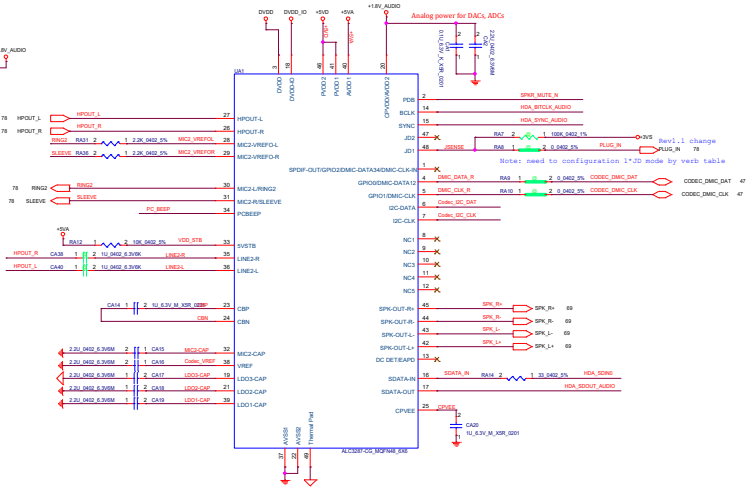
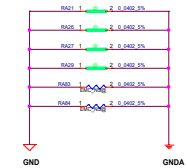
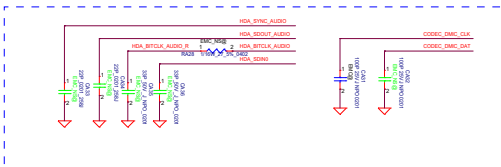
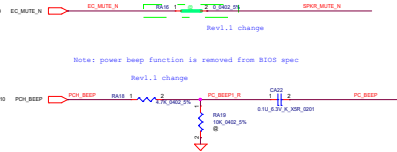
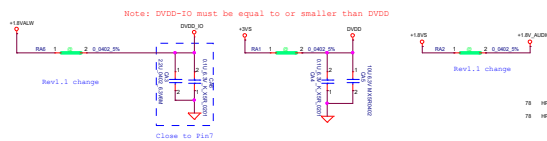
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				C	Y540
				Rev	40
Date				Monday, November 25, 2021	Sheet 64 of 119







- 13 HDA\_BTCLK\_AUDIO
- 13 HDA\_SYNC\_AUDIO
- 13 HDA\_SDOUP\_AUDIO
- 13 HDA\_SDRNG



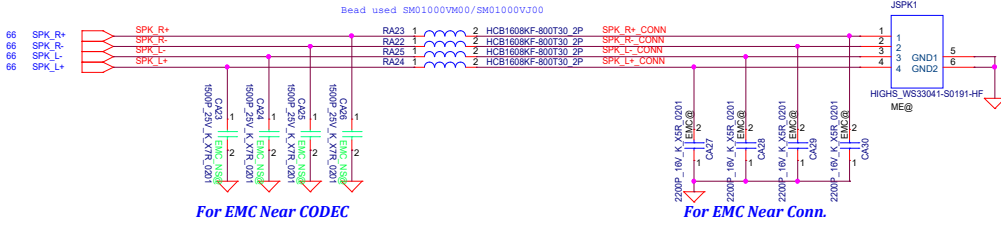
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LCFC Highly Confidential Information			
Issued Date	2013/07/01	Declassified Date	2014/07/01
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Audio Codec ALC3287			

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Rev	C	Document Number	Audio Amplifier		Rev	A0
Scale	Metric, millimeter 1:1		Sheet		87	of 110



Speaker

Speaker



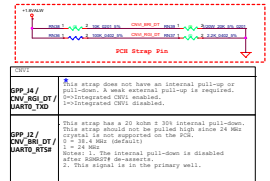
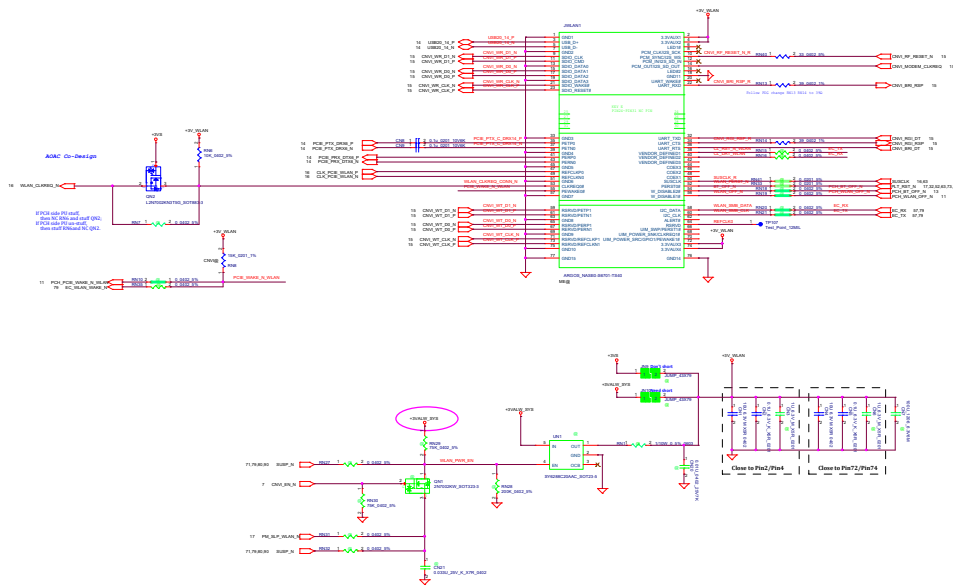
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Audio SPK/Jack

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				Scale	Monday, November 25, 2021
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# Mini-Express Card(WLAN/WiMAX)

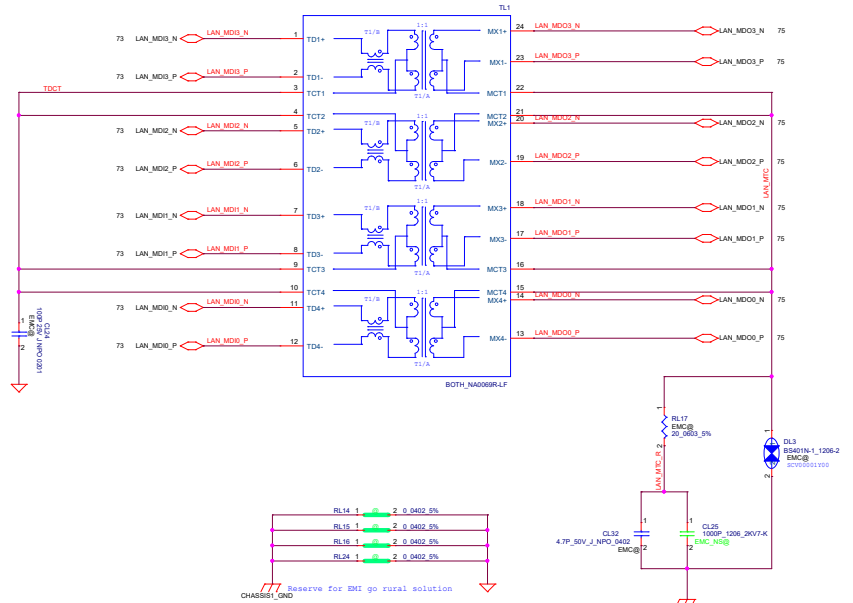
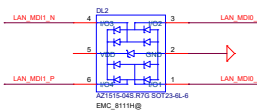
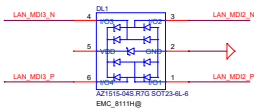


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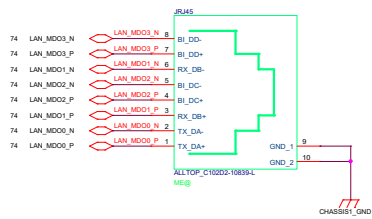


DL1/DL2  
1'S PN:SC300005900  
Place Close to TL1



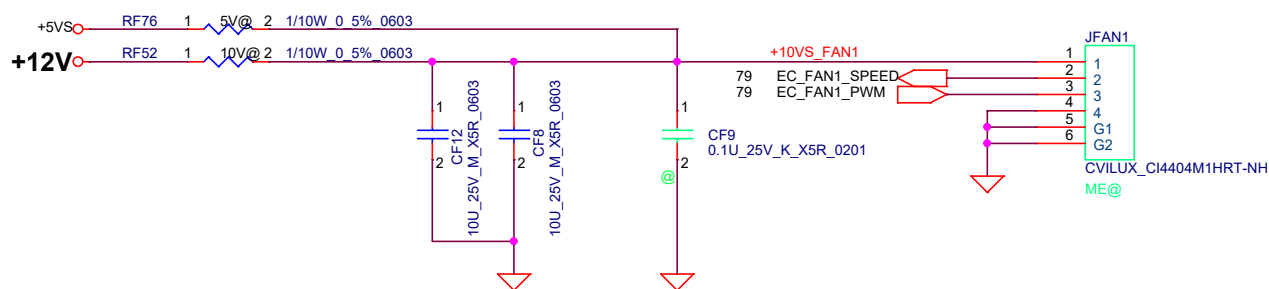
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Issued Date	2019/07/02	Deciphered Date	2020/02/24	DC V TO VS INTERFACE	
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				Sheet	75 of 110

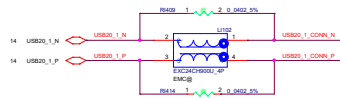




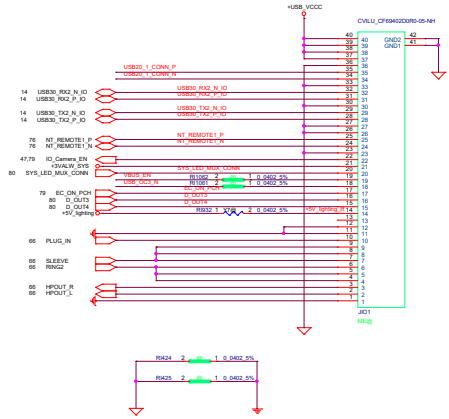
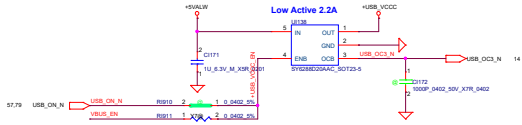
The schematic diagram illustrates the fan speed control circuit. It features a +12V input connected to two voltage regulators: RF77 (5V) and RF75 (10V). The 5V output of RF77 is connected to the EC\_FAN2\_SPEED pin of the JFAN2 module. The 10V output of RF75 is connected to the EC\_FAN2\_PWM pin of the JFAN2 module. The JFAN2 module is connected to the CVILUX\_Ci4404M1HRT-NH module, which has pins for G1, G2, and ME@.

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						A		Y540		A0	
5		4		3		Date:		Monday, November 29, 2021		Sheet 77 of 110	
						2		1			

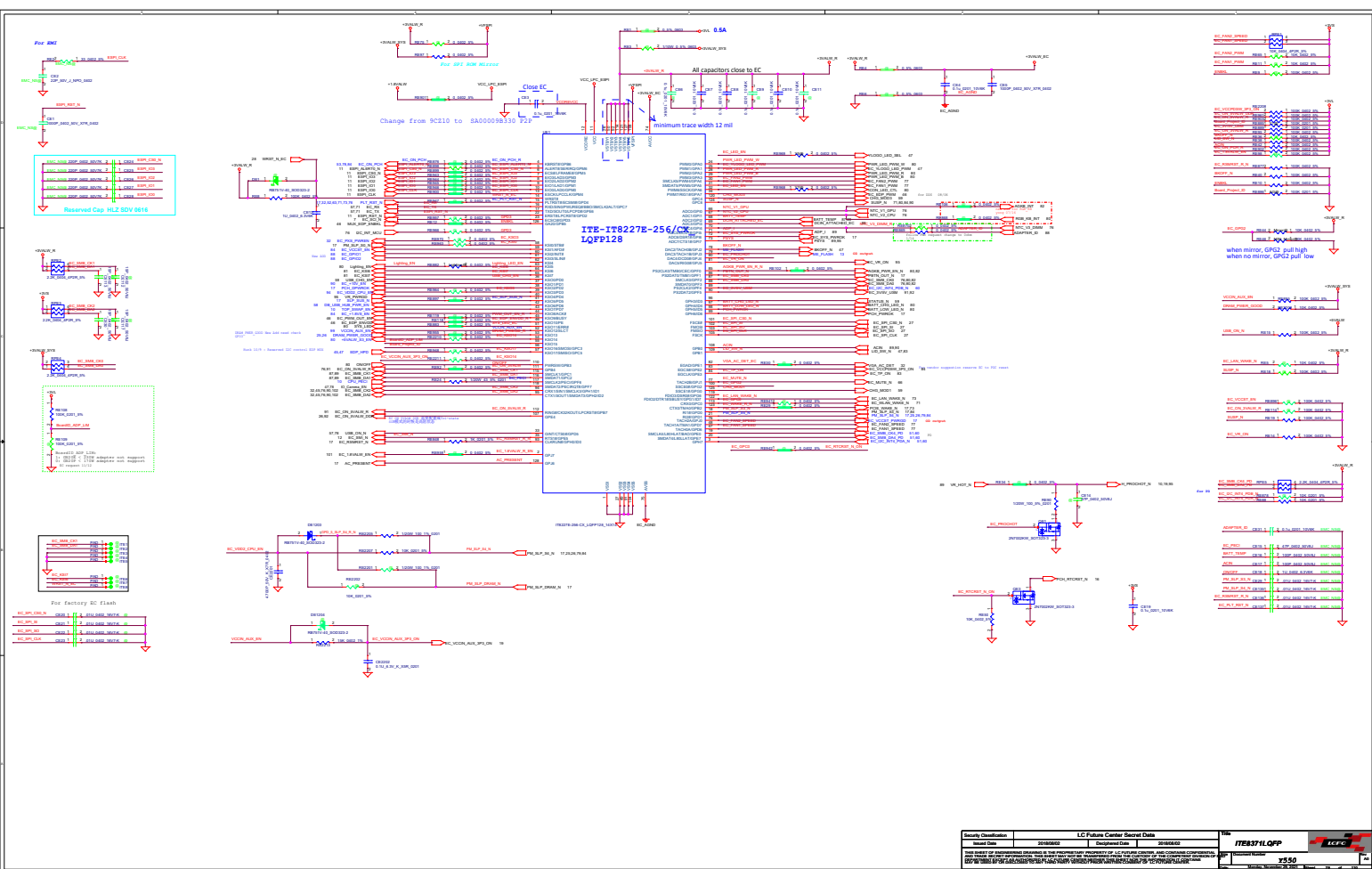
Right Side USB2.0 Port X1 (USB/B)



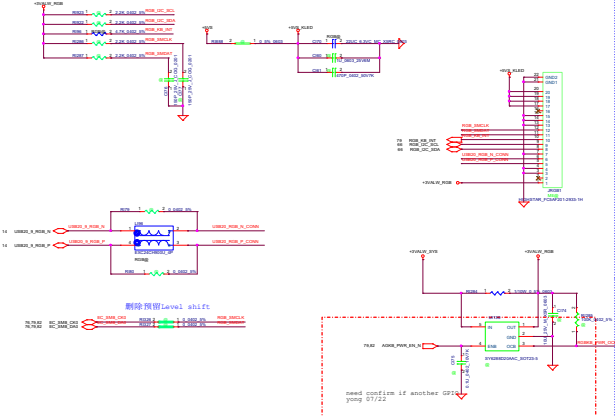
USB3.1 PORT x1



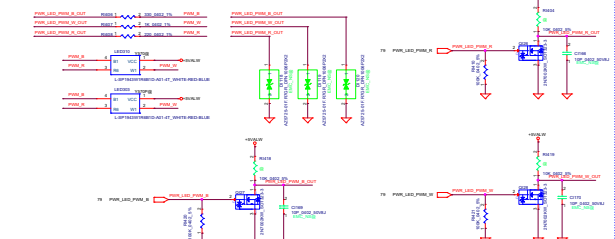
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Module Number: 28, 2021		78		118	
Date		Sheet		of	



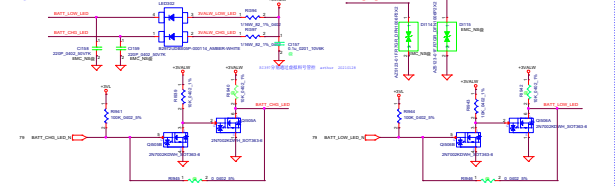
for Y560 KB lighting  
04/27



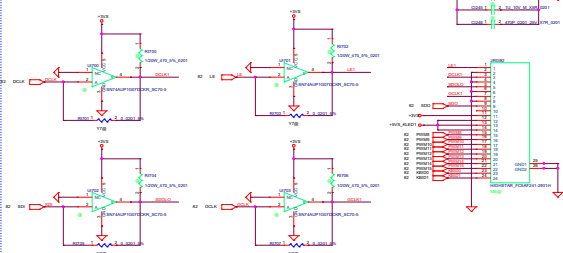
Power Button LED



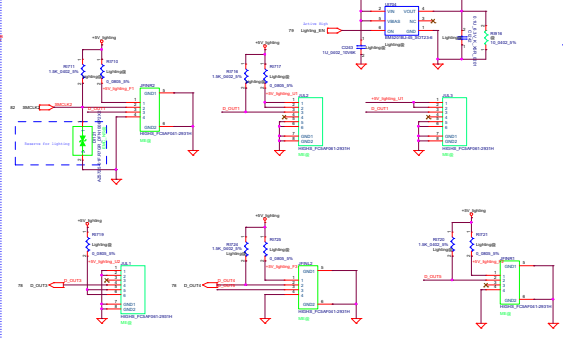
Charger LED



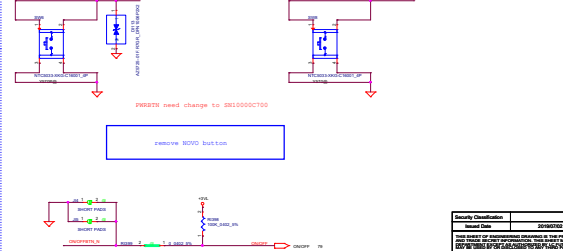
for Y760 KB lighting  
04/27



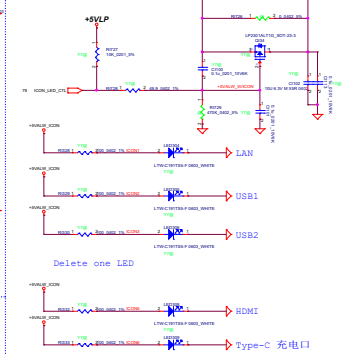
for Y760 system lighting  
04/27



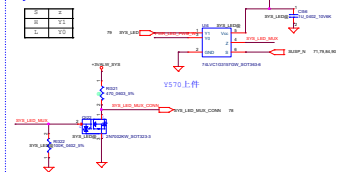
ON/OFF switch



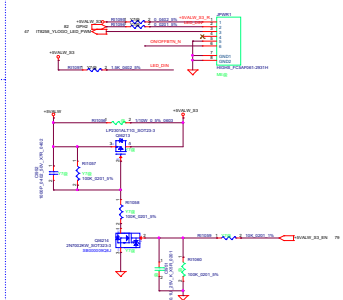
for rear side ICON LED



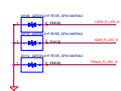
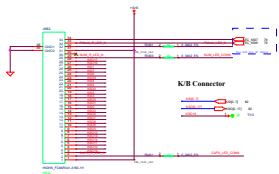
system LED



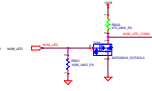
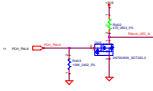
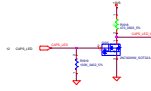
Power button for Y770



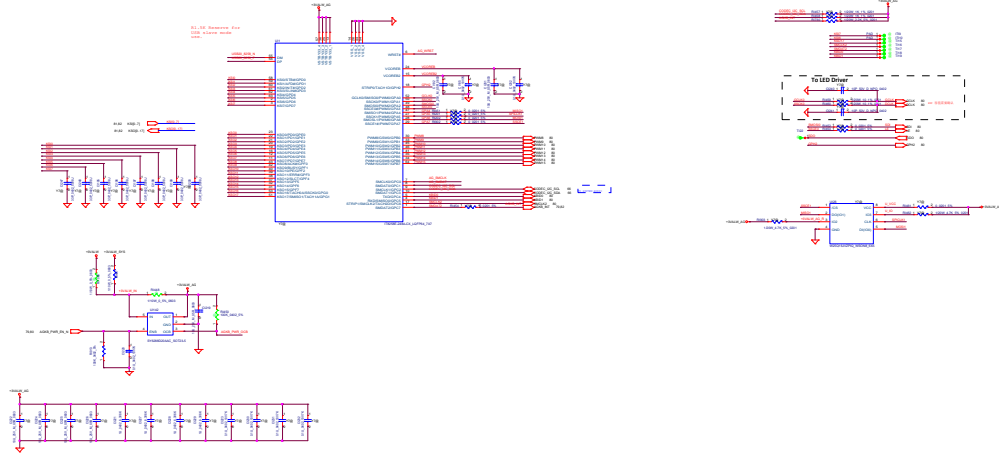




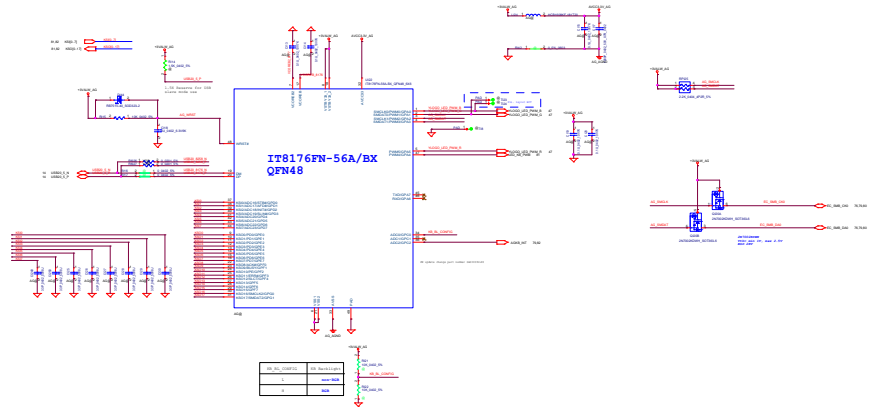
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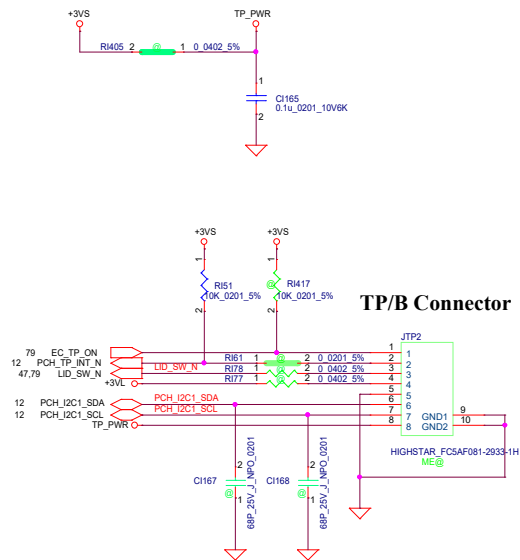
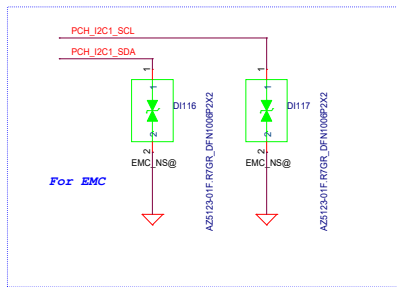



IT8258

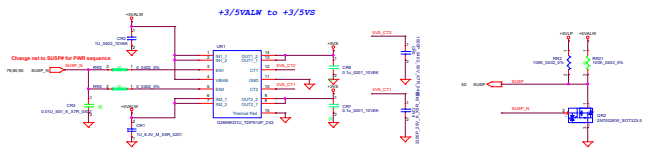


IT8176

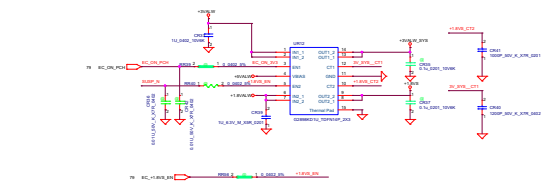
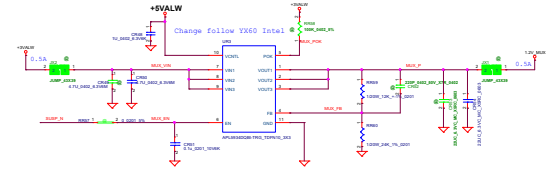




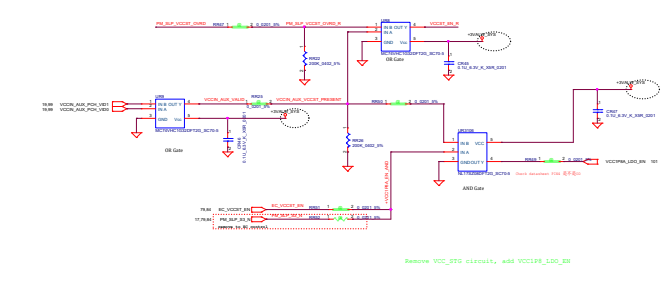
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For Parade 1.2V

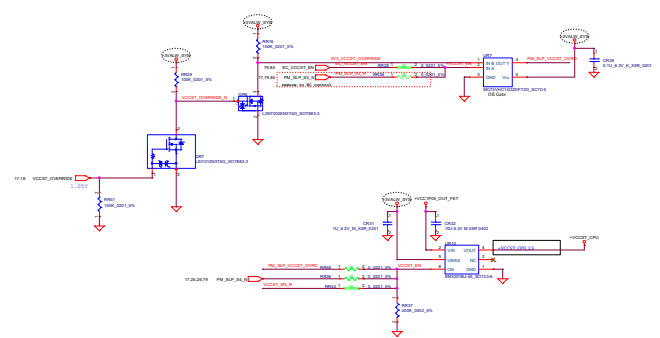



For +VCCP08N\_3F3

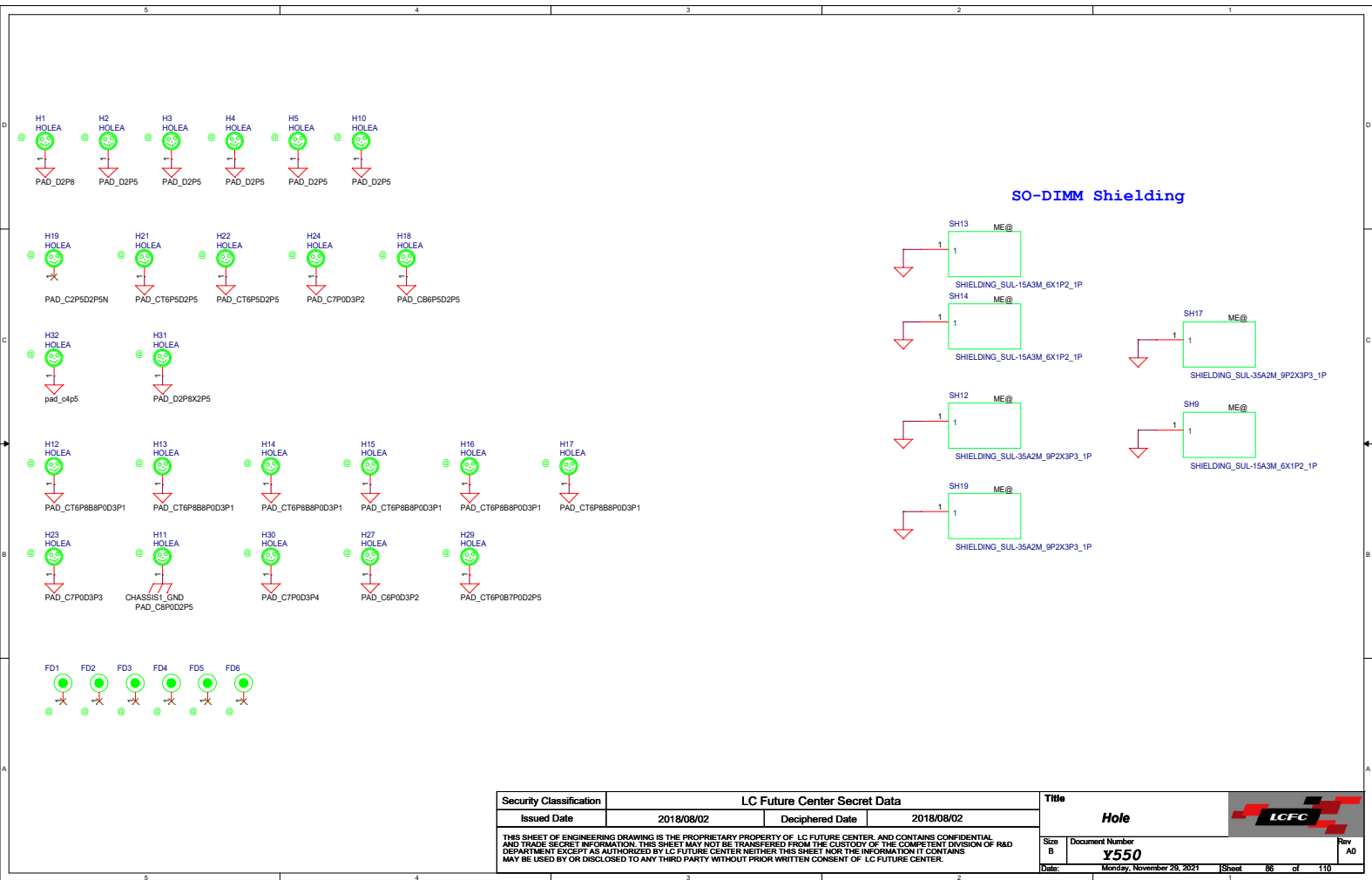



Remove VCC\_0V0 circuit, add VCCP08N\_3F3

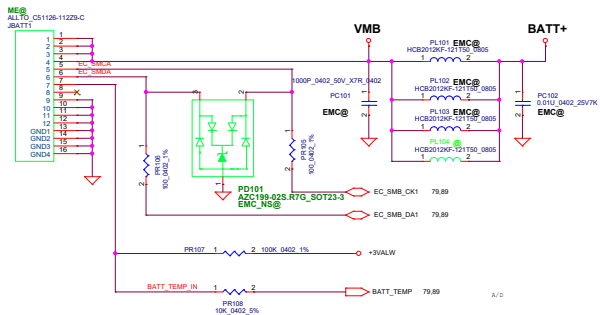
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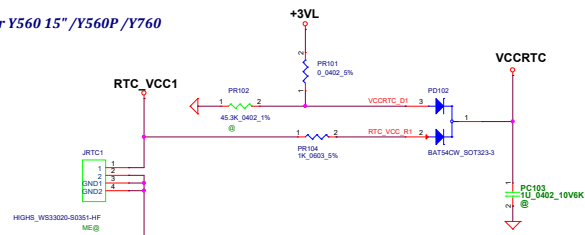
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For Y560 15"/Y560P/Y760



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		Y560		Rev	
		Monday, November 26, 2021		Sheet 87 of 110	





ACDET Threshold:min:17.878V  
BAT Max V=17.6V

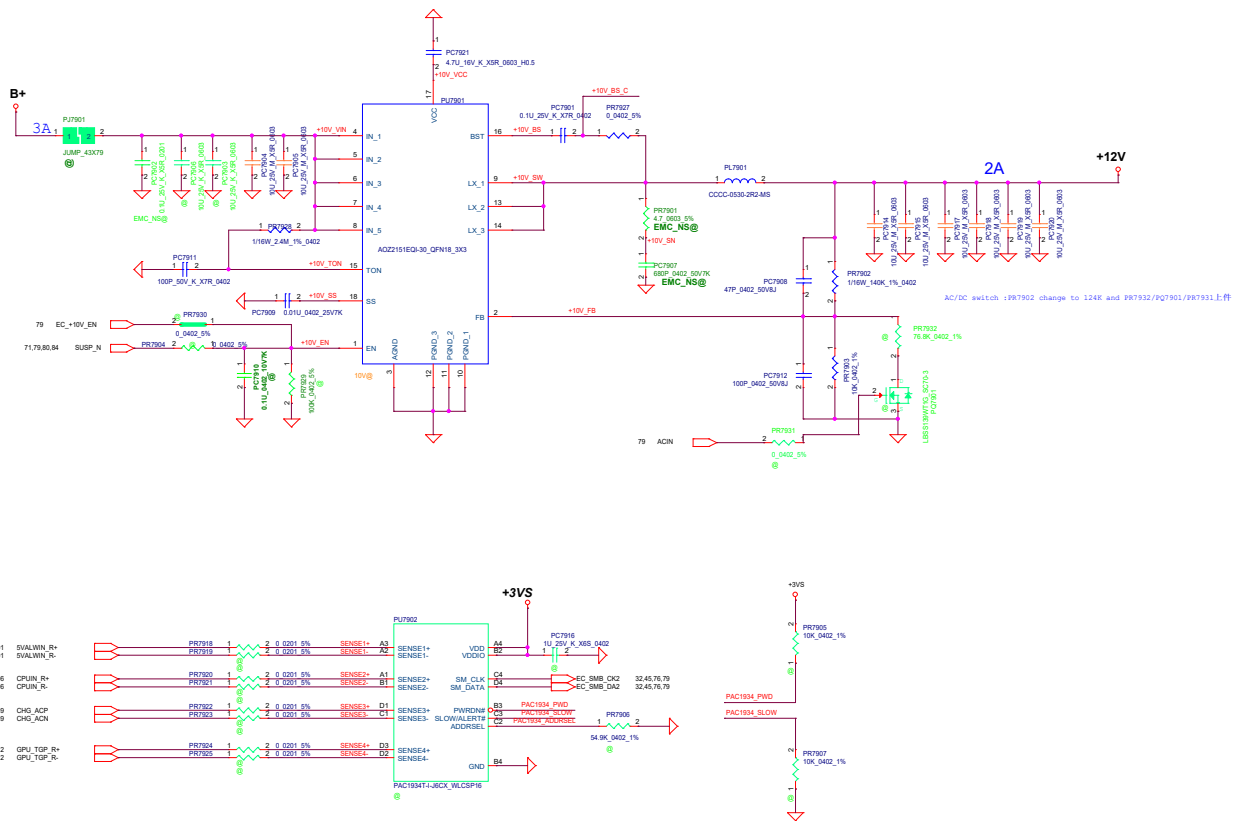
PMON Gain=1uA/W Actuel=0.5uA/W  
PR5415=15K 0.75V=100W

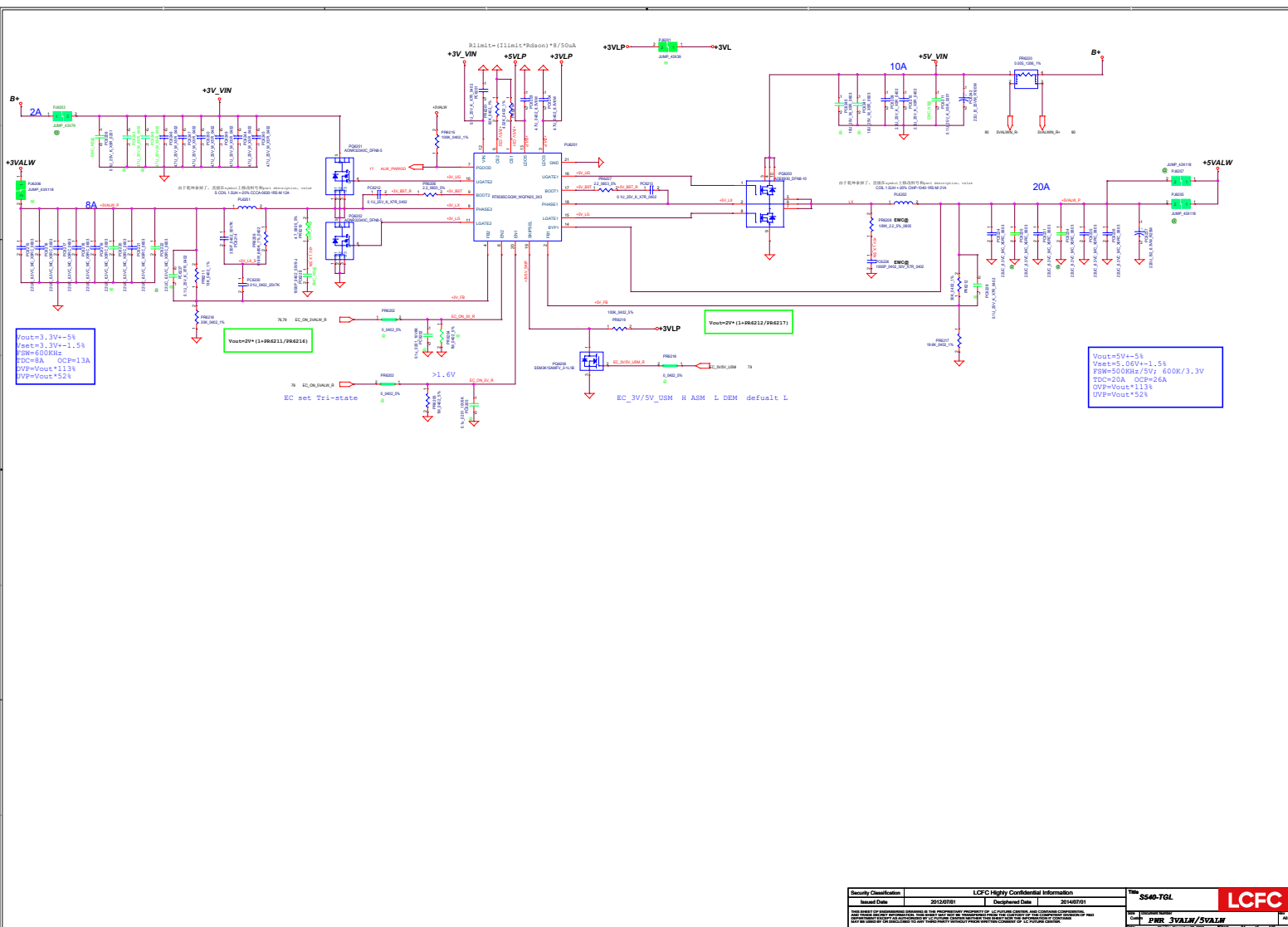
IchargeLIM=17.6A  
IPLchargeLIM=70.4A

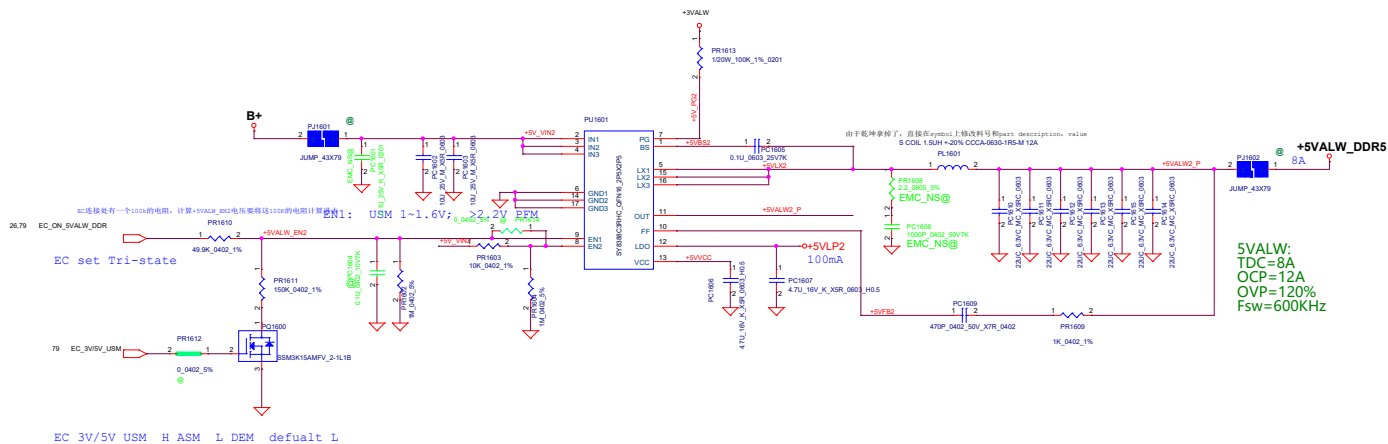
For Charge current ~16A


V charge (MAX):17.6V  
I charge (MAX):16A  
FSW:500K

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Issued Date	2018/08/02	Disphanded Date	2018/08/02	PWR-charger	
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				Rev	01
				Rev	01







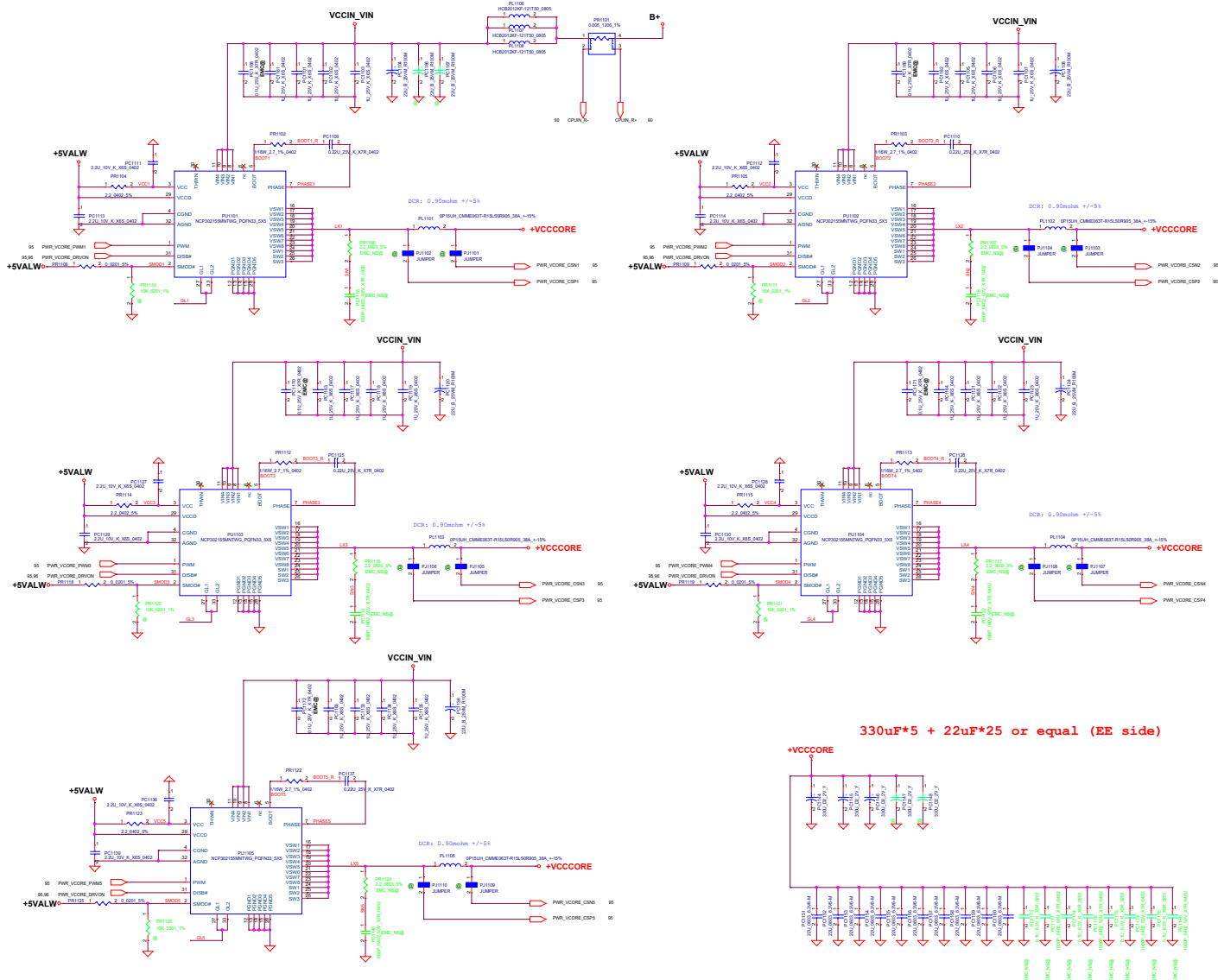
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<small>Issue</small> Monday, November 28, 2017				<small>Scale</small> 95 of 118



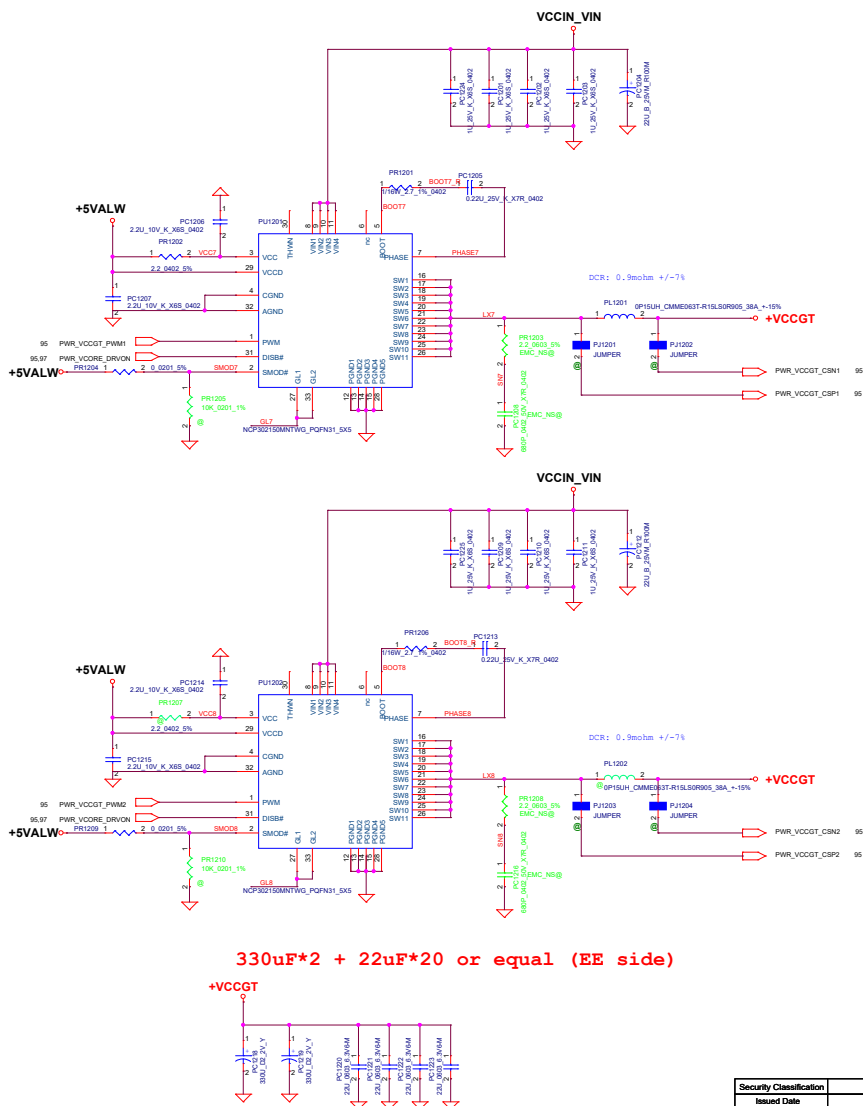






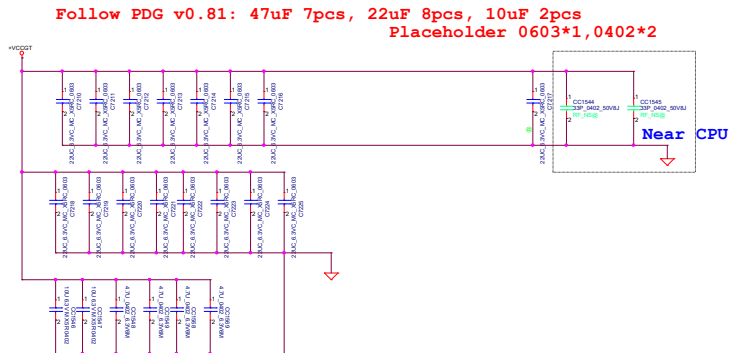
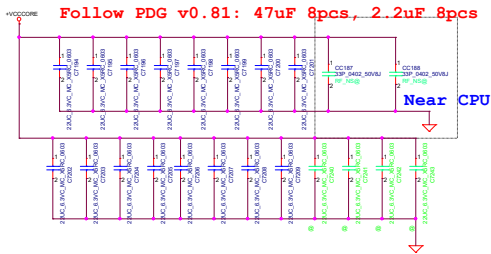
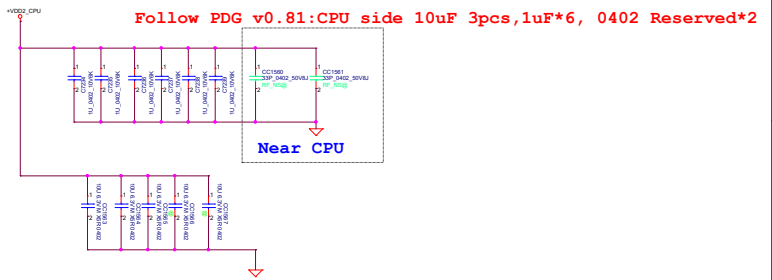
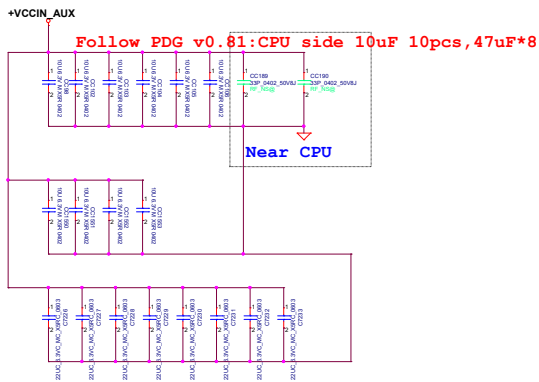
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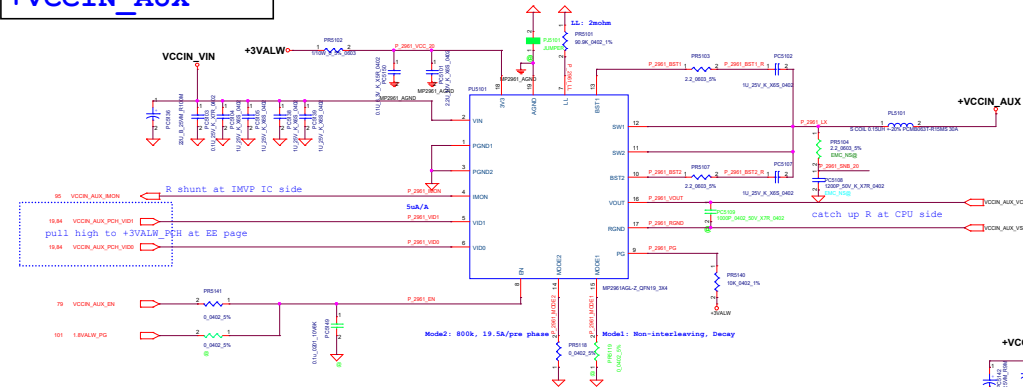
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Date	Monday, November 25, 2013		Rev		1.0

# +VCCIN\_AUX



Part	Value	Unit	Notes
R1	100k	Ω	100kΩ
R2	10k	Ω	10kΩ
R3	1k	Ω	1kΩ
R4	100k	Ω	100kΩ

Part	Value	Unit	Notes
C1	100nF	F	100nF
C2	10uF	F	10uF
C3	100uF	F	100uF
C4	10k	Ω	10kΩ

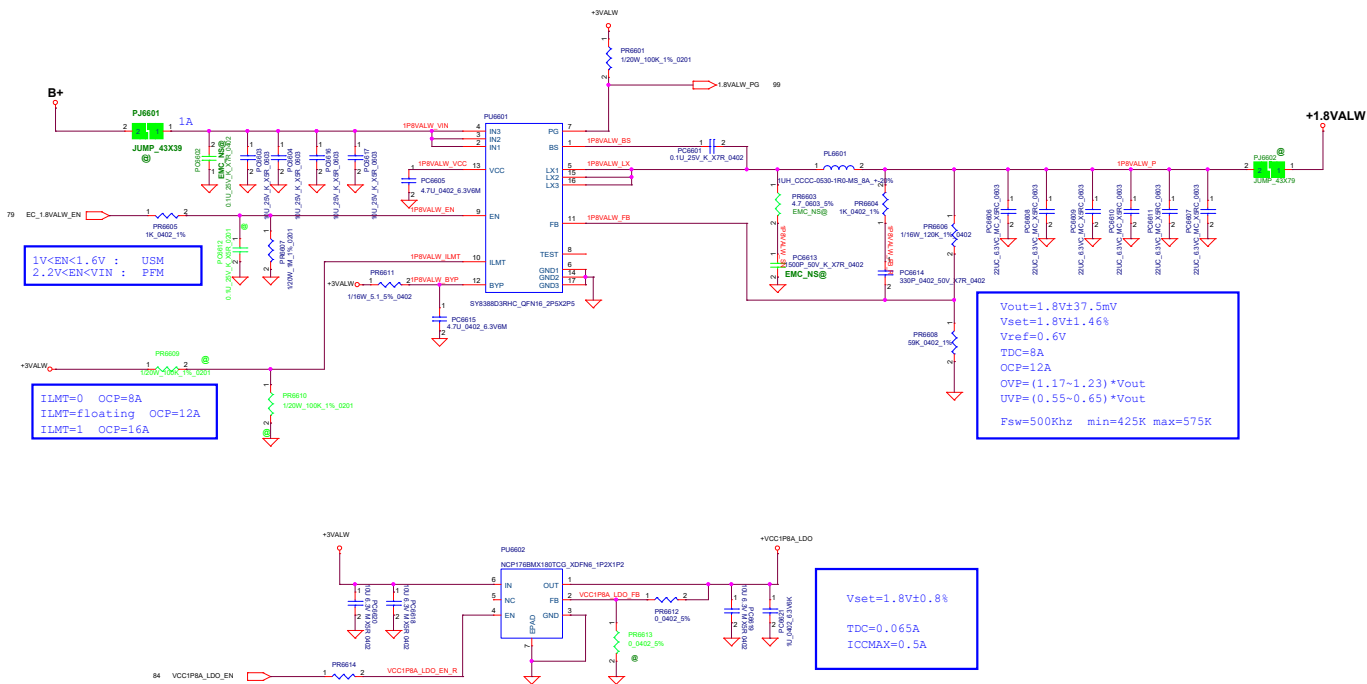
Part	Value	Unit	Notes
R1	100k	Ω	100kΩ
R2	10k	Ω	10kΩ
R3	1k	Ω	1kΩ
R4	100k	Ω	100kΩ

Part	Value	Unit	Notes
C1	100nF	F	100nF
C2	10uF	F	10uF
C3	100uF	F	100uF
C4	10k	Ω	10kΩ

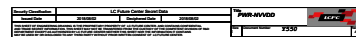
330uF\*1 + 22uF\*18 or equal (EE side)

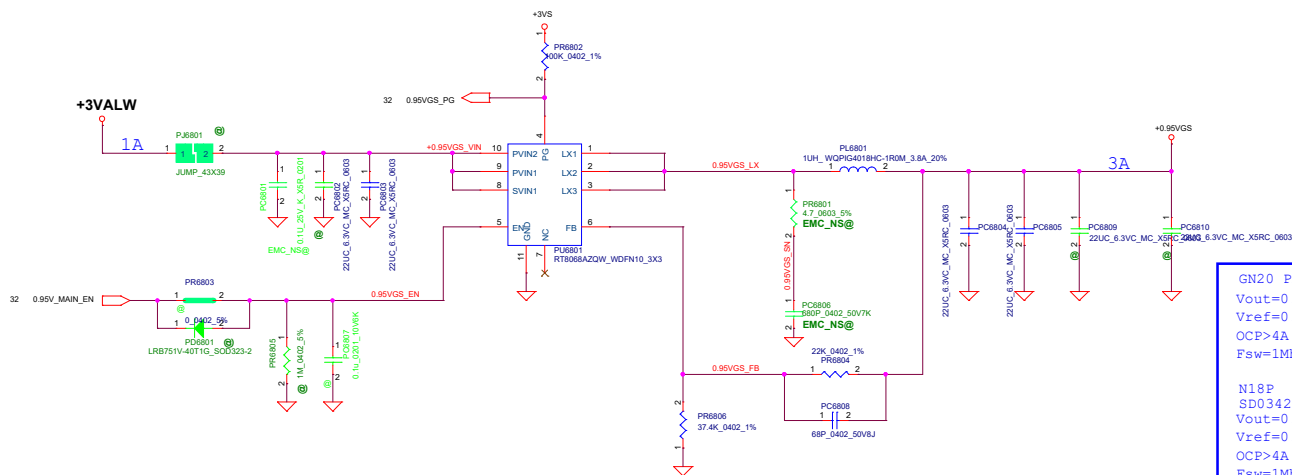


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				LCFC	
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X560				AMD	
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GN20 PR6804=22K  
 Vout=0.953V±3%  
 Vref=0.6V  
 OCP>4A  
 Fsw=1Mhz

N18P PR6804=26.1K  
 SD03426128J  
 Vout=0.953V±3%  
 Vref=0.6V  
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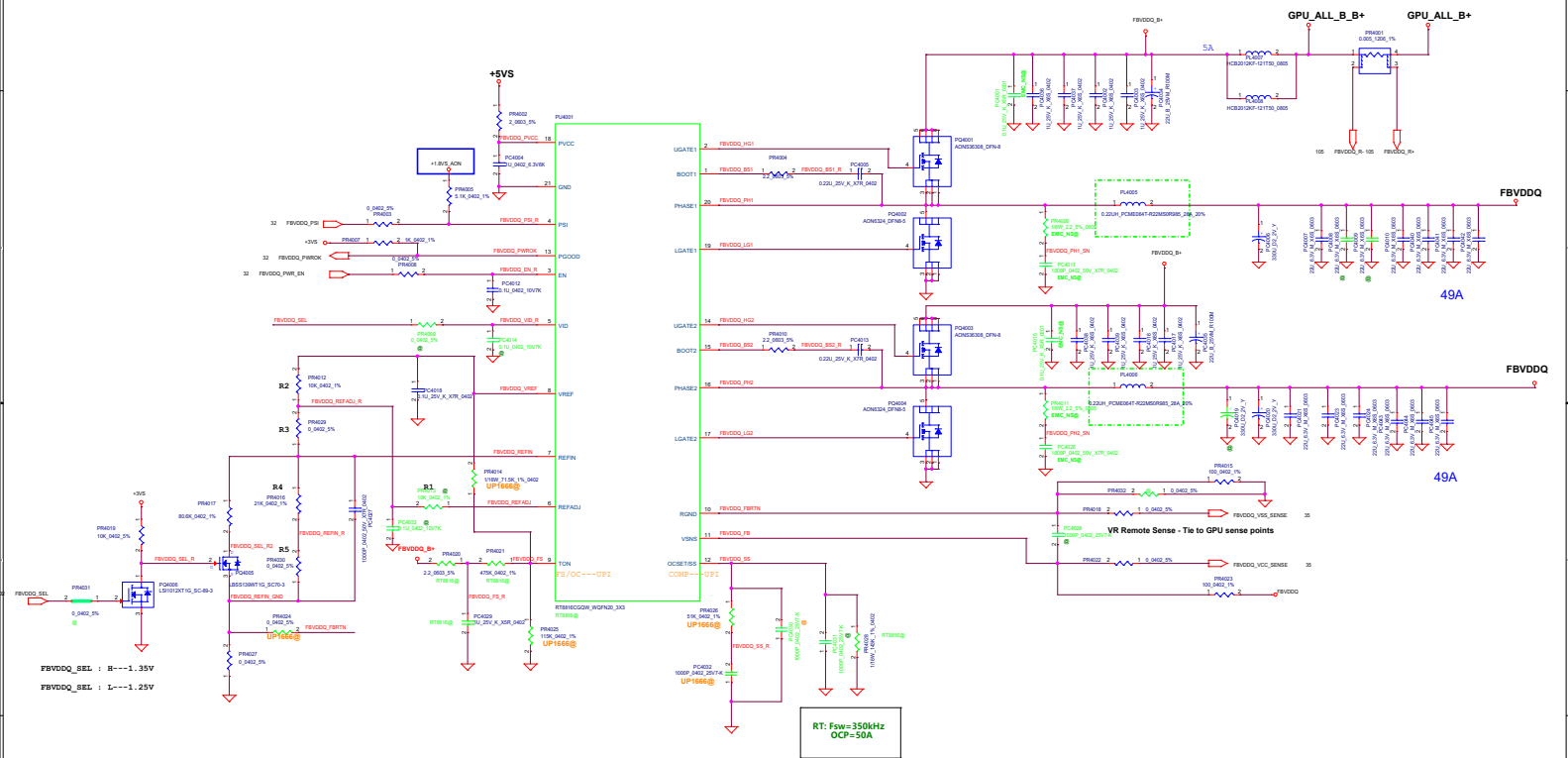
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RT8816 PSI	UP1666 PSI	Phase Configuratio
1.6V~5.5V	1.6~5.5V	2Phase CCM
1.08~1.35V	1~1.4V	2Phase DEM
0.7~0.88V	0.4V~0.8V	1Phase CCM
0~0.4V	0~0.2V	1Phase DEM



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				C	<b>Y560 AMD</b>	A0
				Doc	Revision: November 25, 2021	Sheet 119 of 119